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# MS-7759

m-ATX

H/W:Kevin Lin

Ver: 1.0(243.84 \* 243.84)

PM:Aaron

## Intel -MahoBay platform Z77

### CPU:

IVY bridge LGA1155

### System Chipset:

Panther Point Z77

### Onboard Chip:

HD Audio Codec:ALC887 colay 892

LAN-RTL8111E colay8105E

SIO:Fintek F71868

Flash ROM: SPI 64 MB

### Main Memory:

DDRIII (1066/1333/1600MHz) \* 4 (Dual Channel)

### ACPI:

UPI

### PWM:

VRD12 -UP1625Q 3+1 Phase

### Expansion Slots:

PCI Express (X16) Slot \* 1

PCI Express (X1 ) Slot \* 2

PCI Express (X8) Slot \* 1

Other: SATA3.0 x2+SATA2.0 x4 (PCH)

USB2.0 \*10

REAL USB3.0 \*2

FRONT USB3.0 \*2

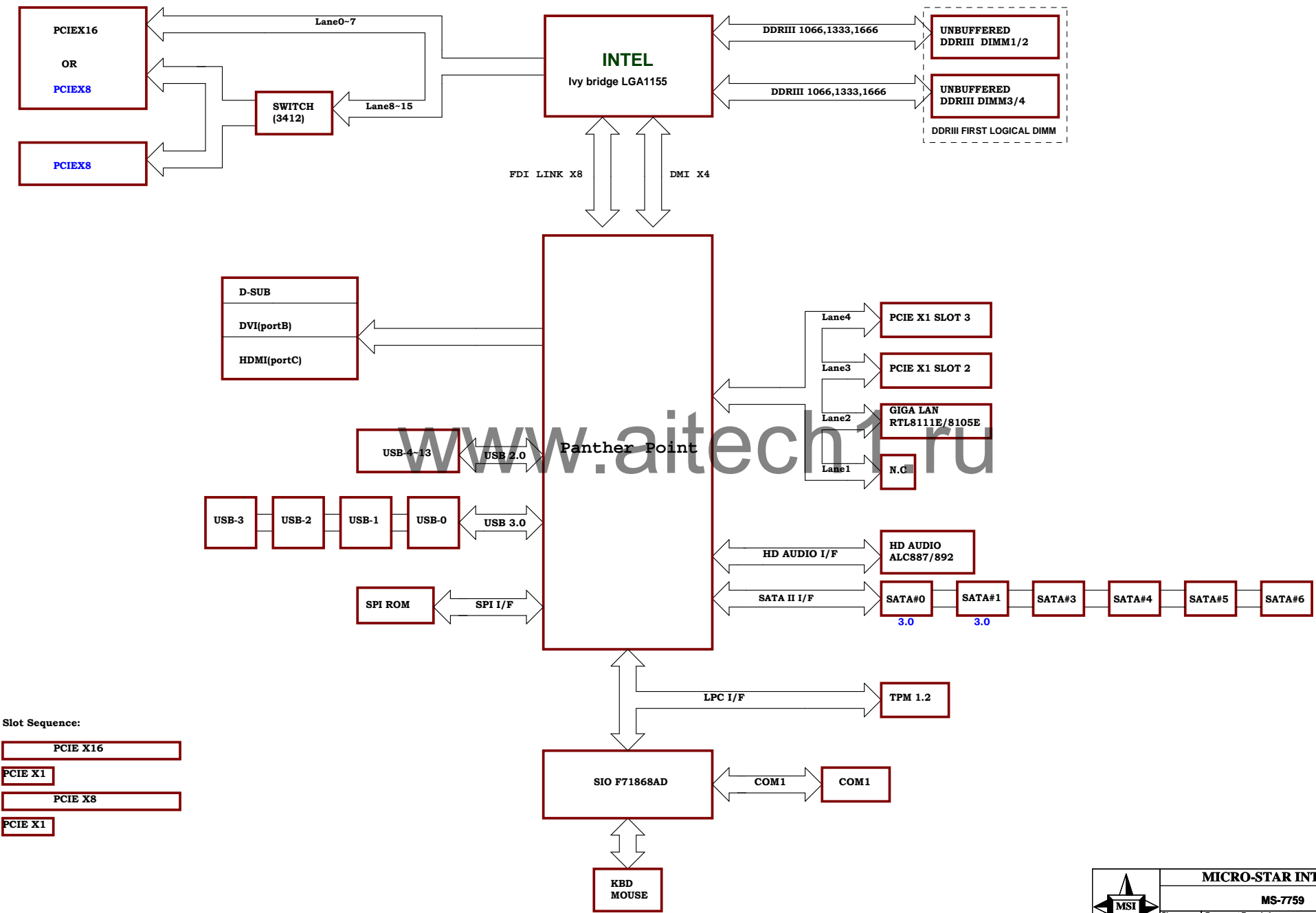


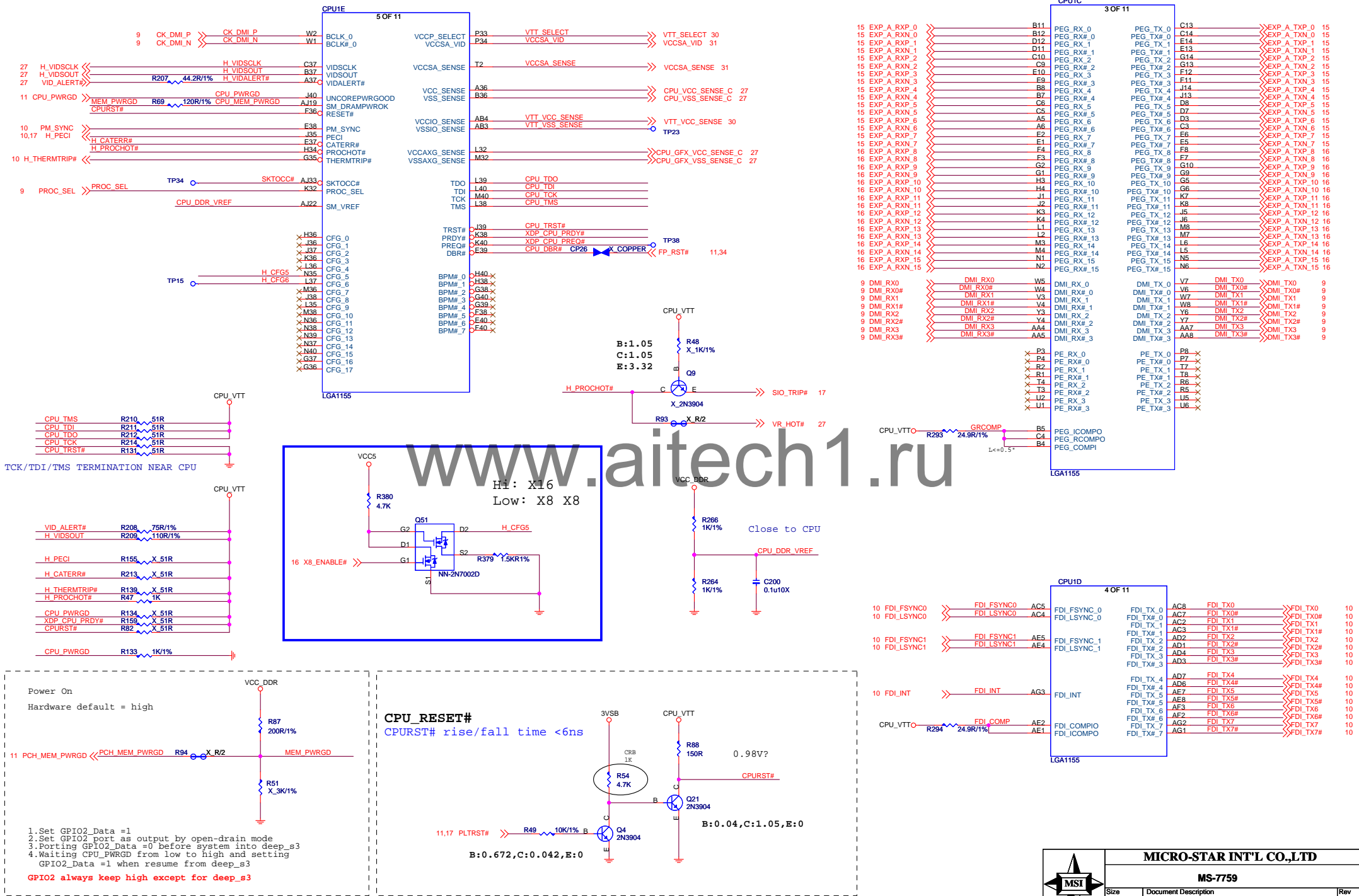
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MS-7759 Block Diagram

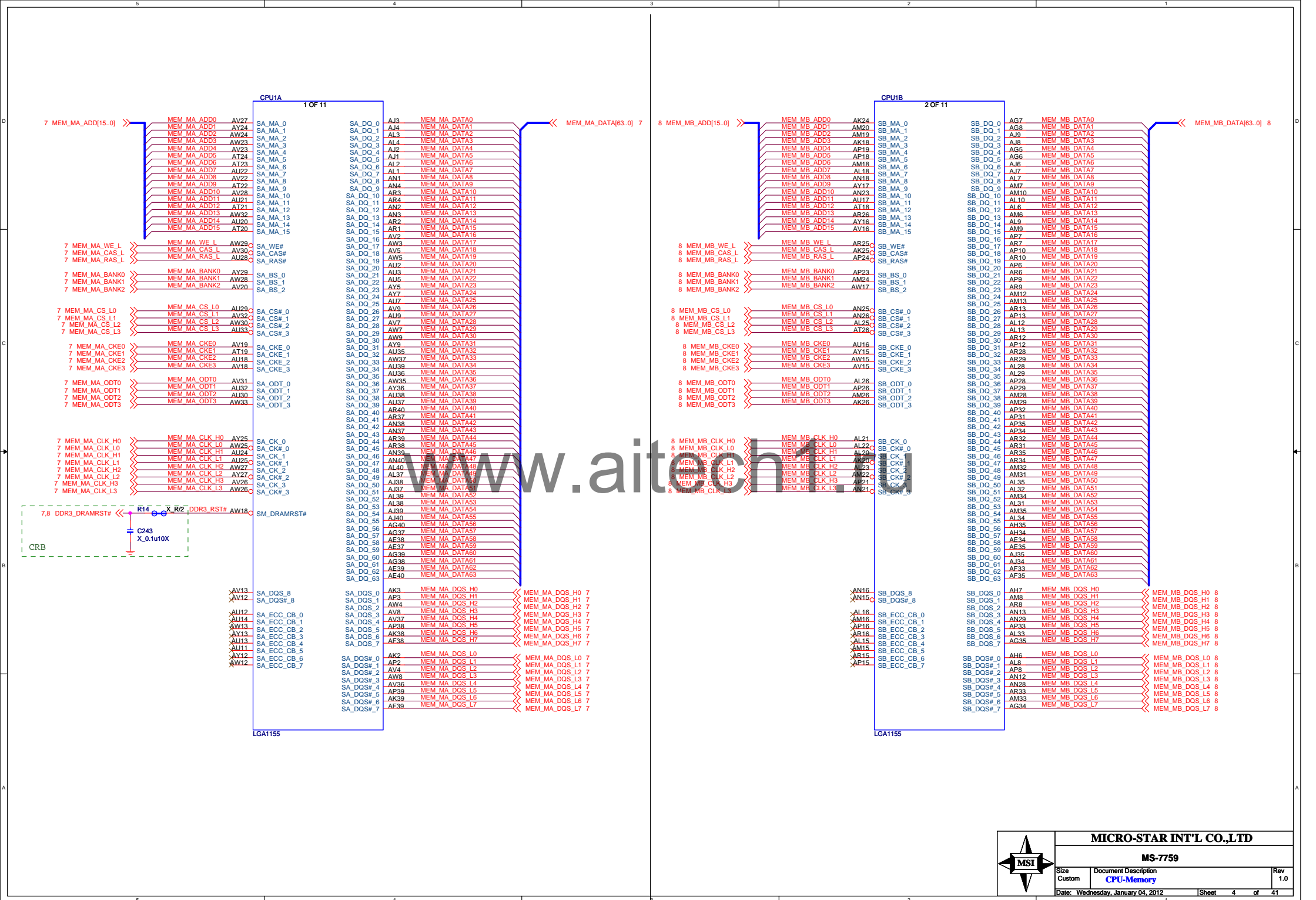


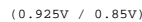
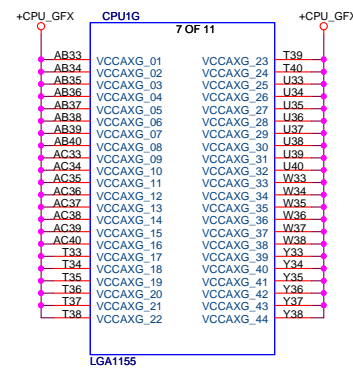
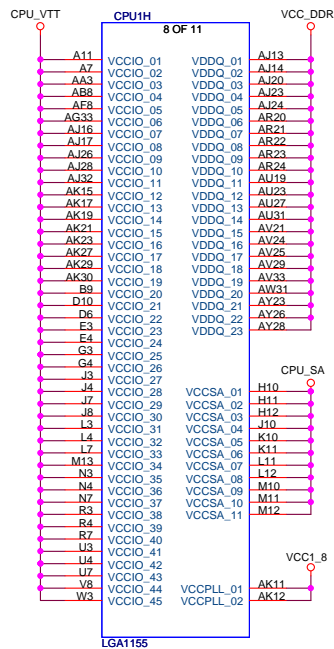
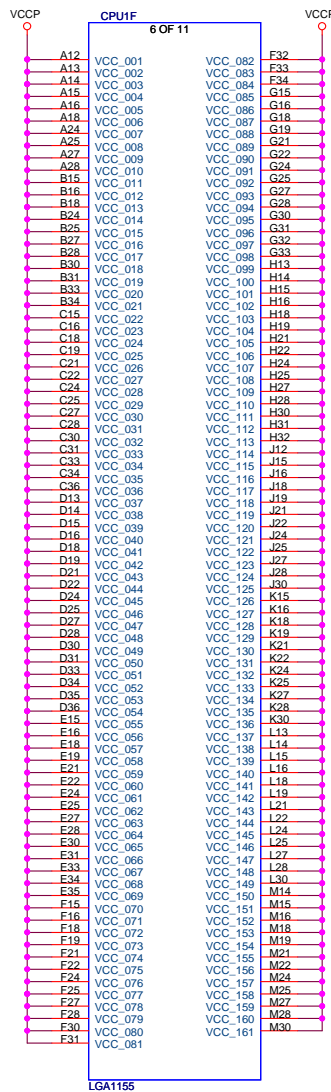


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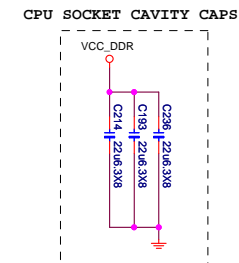
Size	Document Description	Rev
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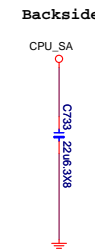


```
VCCP: 112A
CPU_VTT: 8.2A
CPU_SA: 8.8A
VCC_DDR: 4.5A
VCC1_8: 1.6A
```

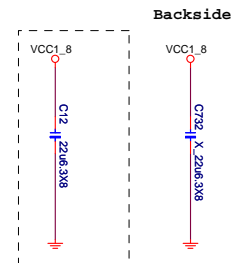
### +1.5V\_DDR3-Decoupling



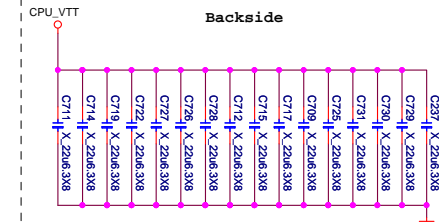
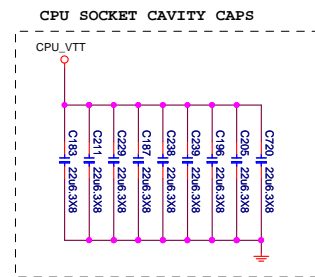
### +CPU\_SA Decoupling



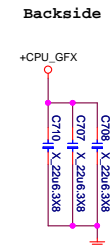
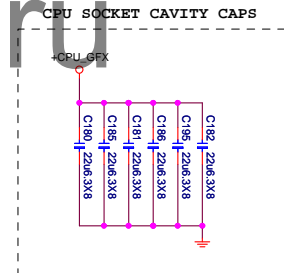
### +VCC1\_8 Decoupling



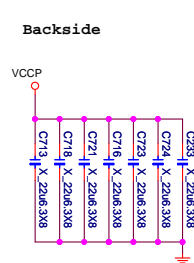
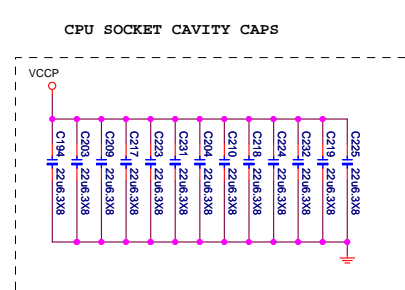
### +CPU\_VTT Decoupling



### +CPU\_GFX Decoupling



### +CPU\_VCCP-Decoupling



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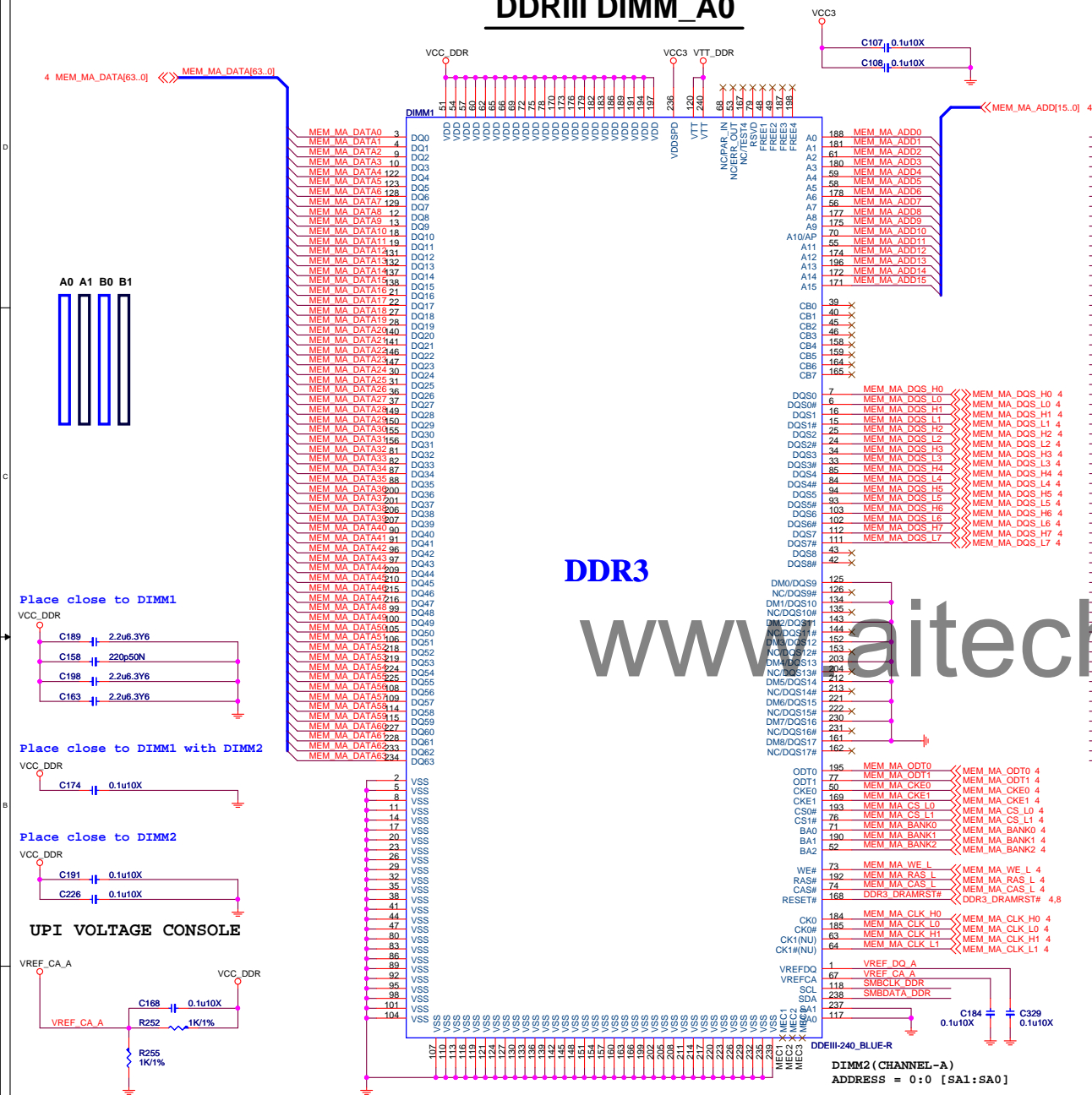
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Size Custom	Document Description <b>CPU-Power</b>	Rev 1.0
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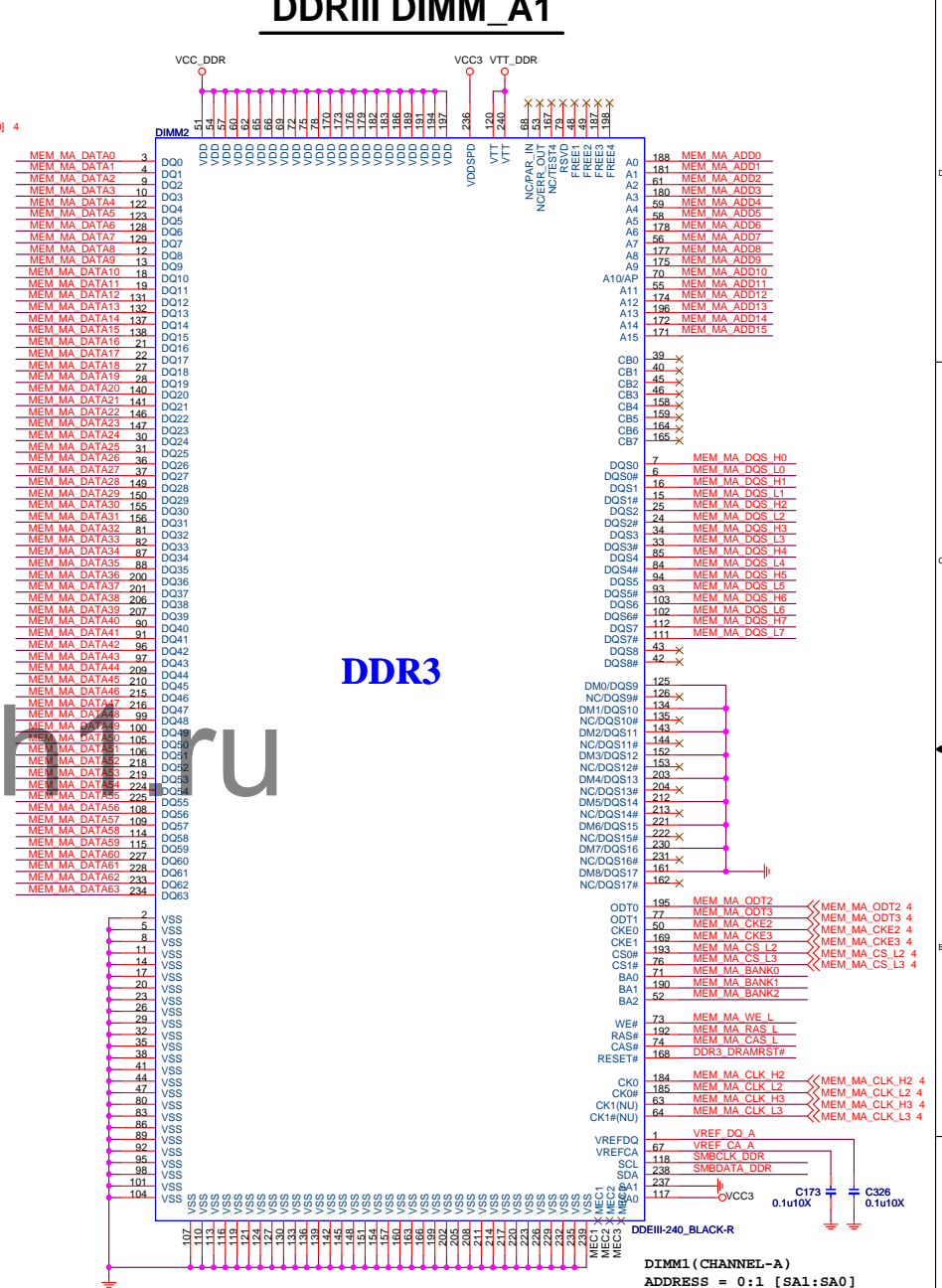


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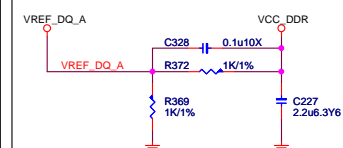
## DDRIII DIMM\_A0



## DDRIII DIMM\_A1



## UPI VOLTAGE CONSOLE

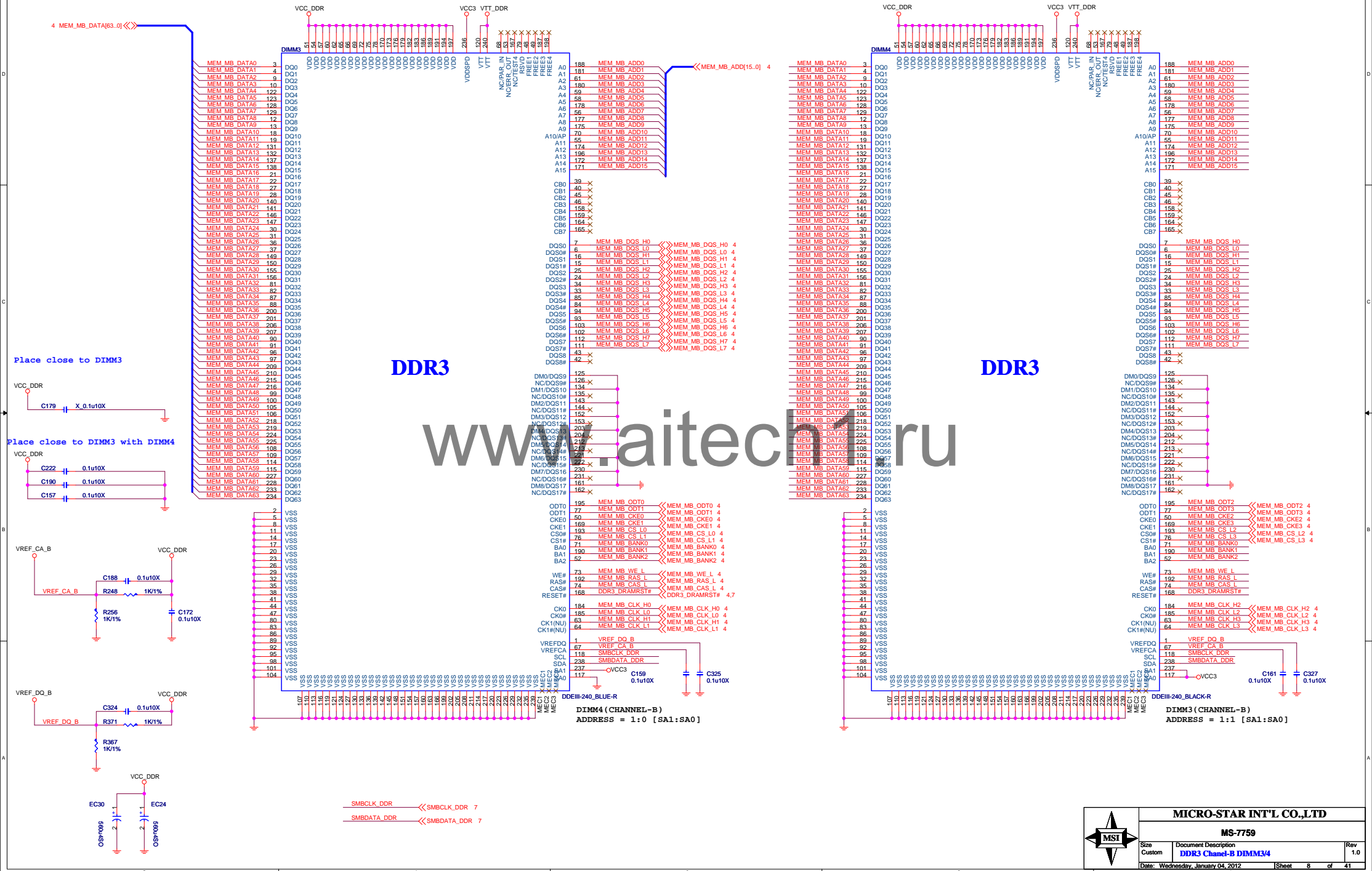


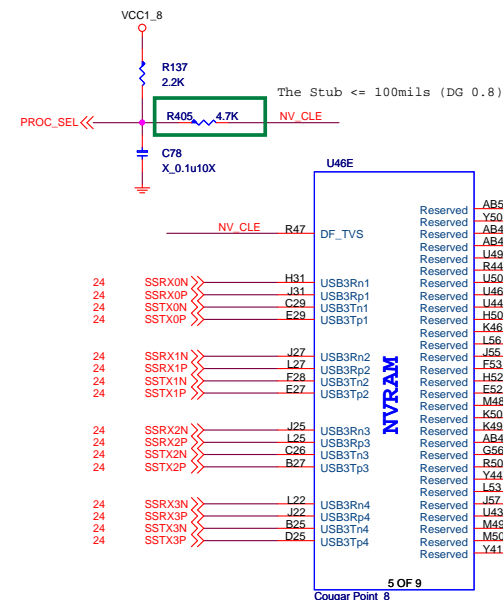
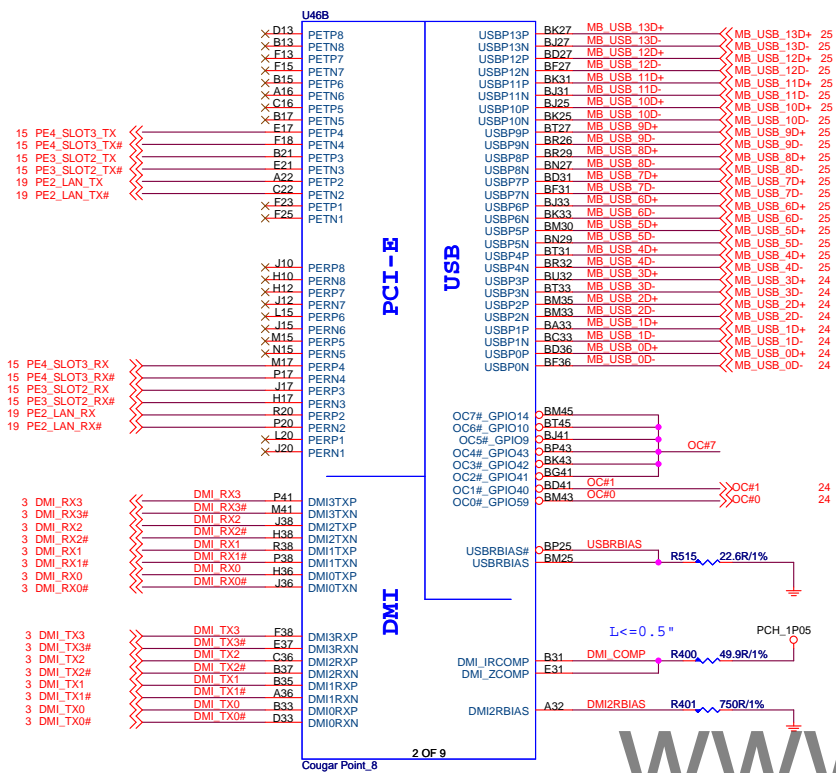
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8 SMBDATA\_DDR >> SMBDATA\_DDR R187 33R << SMBDATA 11,15,16,27,34

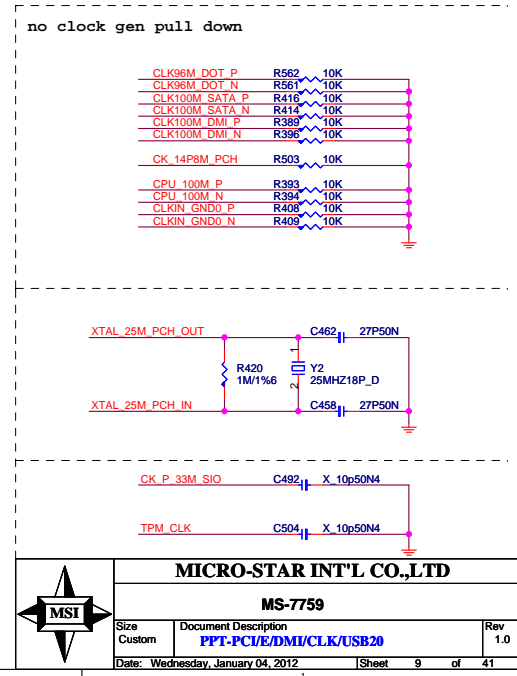
# DDR3 DIMM\_B0

# DDR3 DIMM\_B1

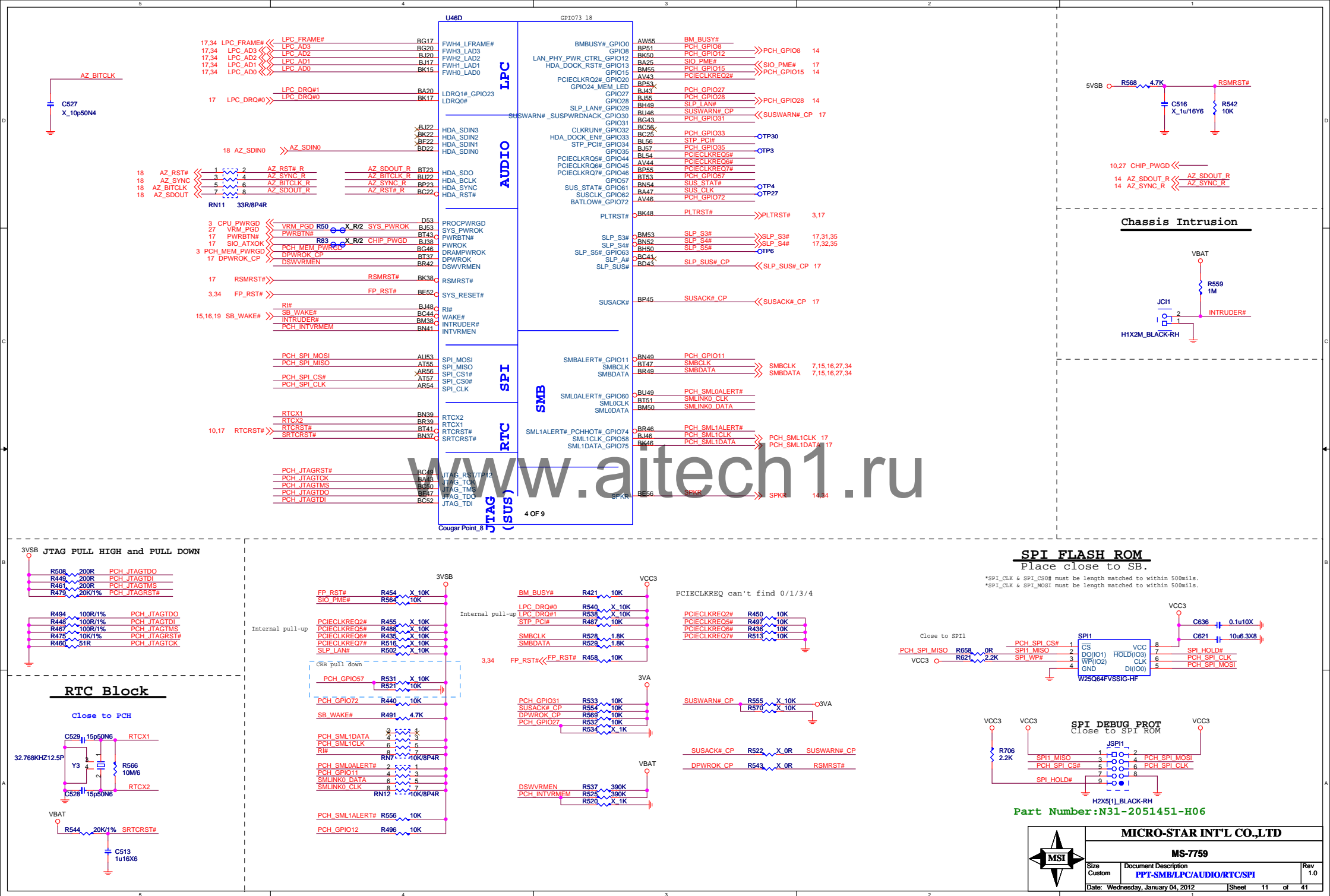




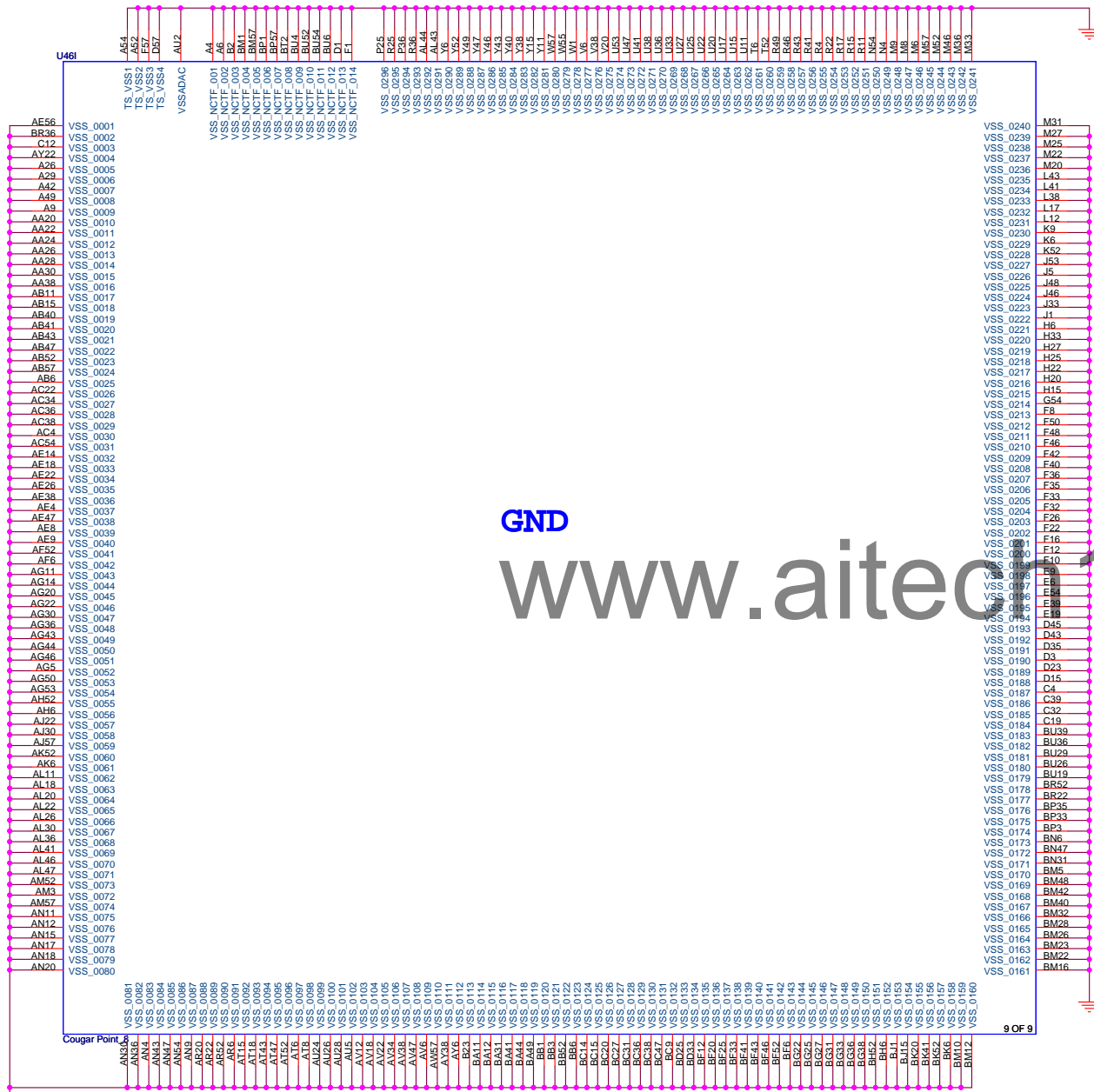
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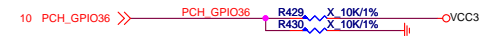
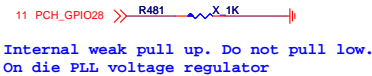
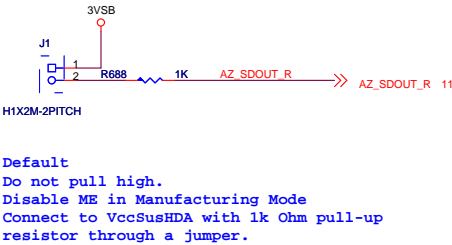
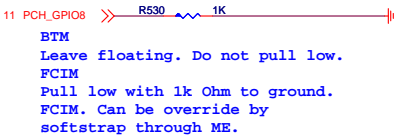
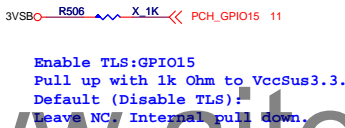
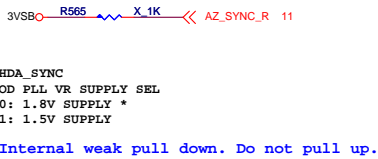
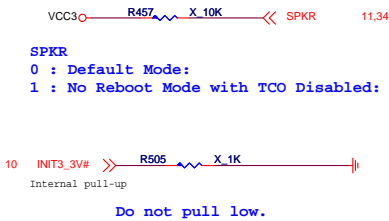








PCH Straps



Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:

a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3\_3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.

b) When Used as GP Input (Pin HW default) - Ensure GPI is not driven high during strap sampling window

When Unused as GPIO or SATA[x]GP - Use 8.2K-10K pull-down to ground.

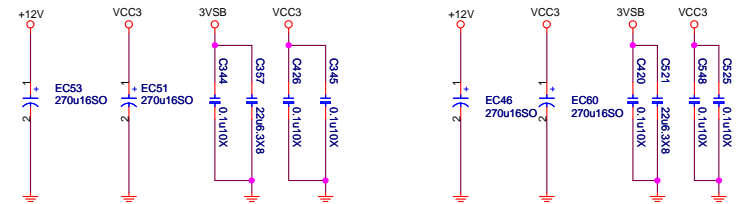
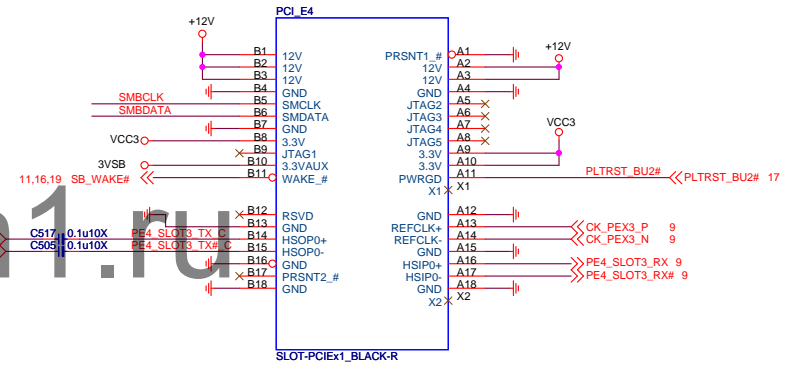
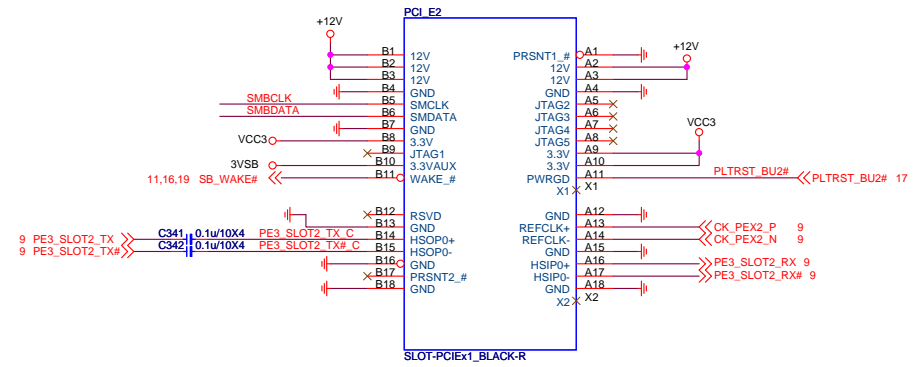


Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:

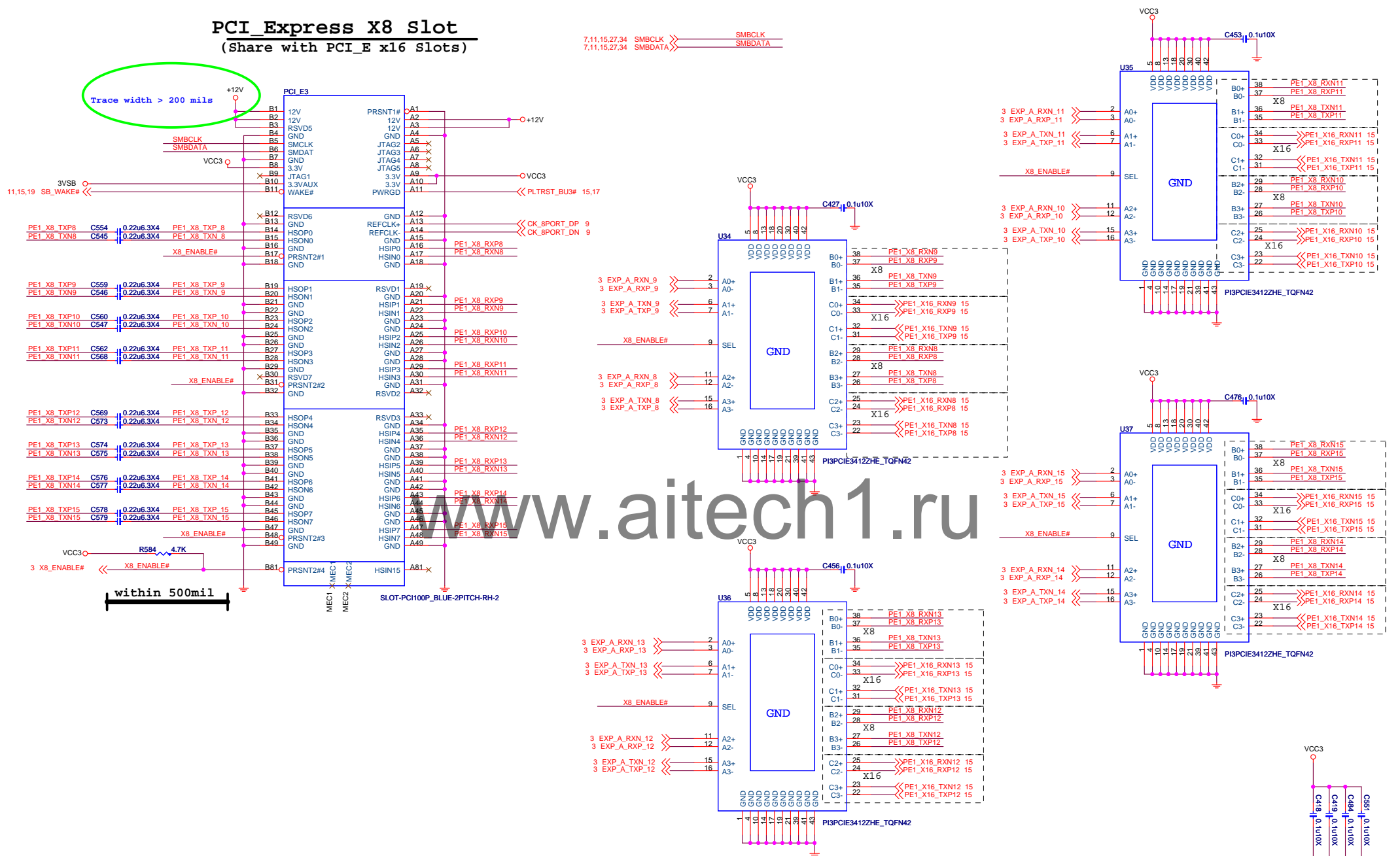
a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3\_3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.

b) When Used as GP Input (Pin HW default) - Ensure GPI is not driven high during strap sampling window


When Unused as GPIO or SATA[x]GP - Use 8.2K-10K pull-down to ground.



# PCI\_Express X8 Slot (Share with PCI\_E x16 Slots)



X8_ENABLE#	PCI-E Slot 1/2
Low	X8 / X8
Hi	X16

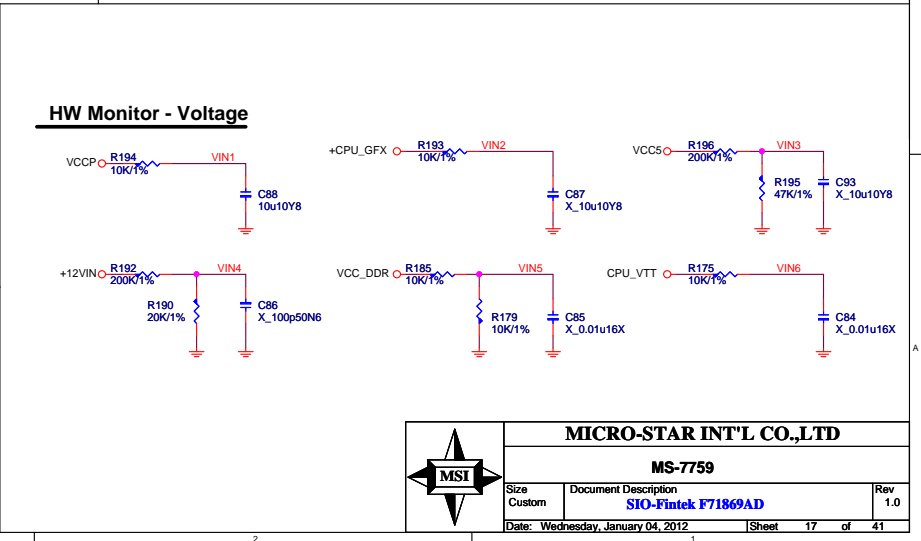
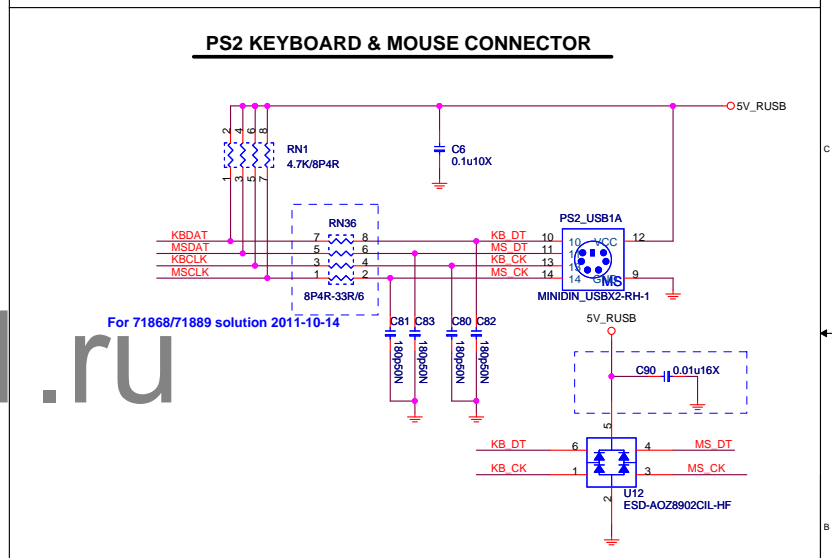


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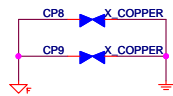
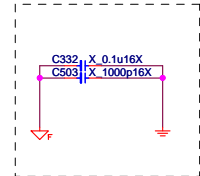
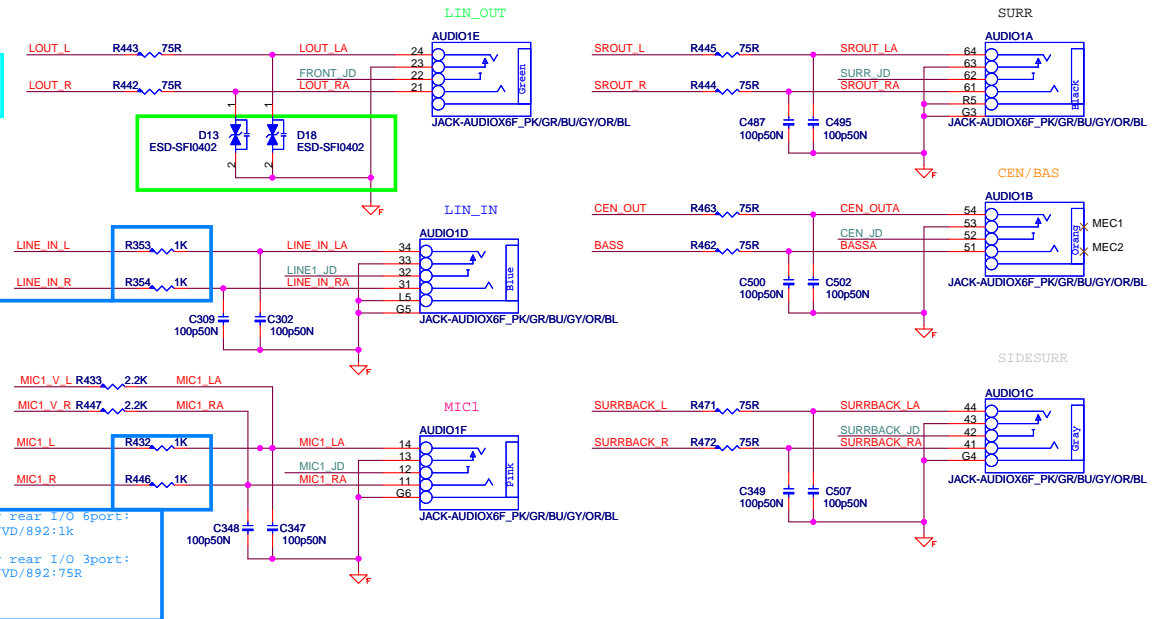
**MS-7759**

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Custom	PCIE5(X8)/Pericom switch	1.0

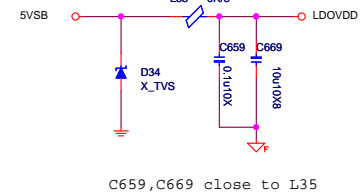
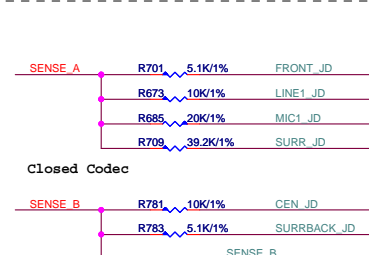
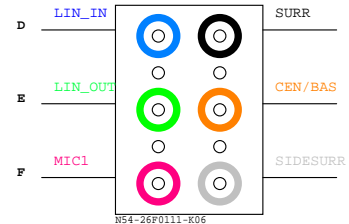
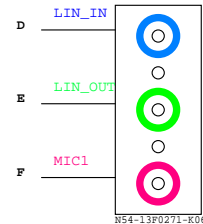
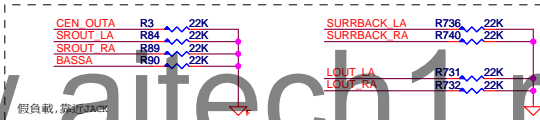
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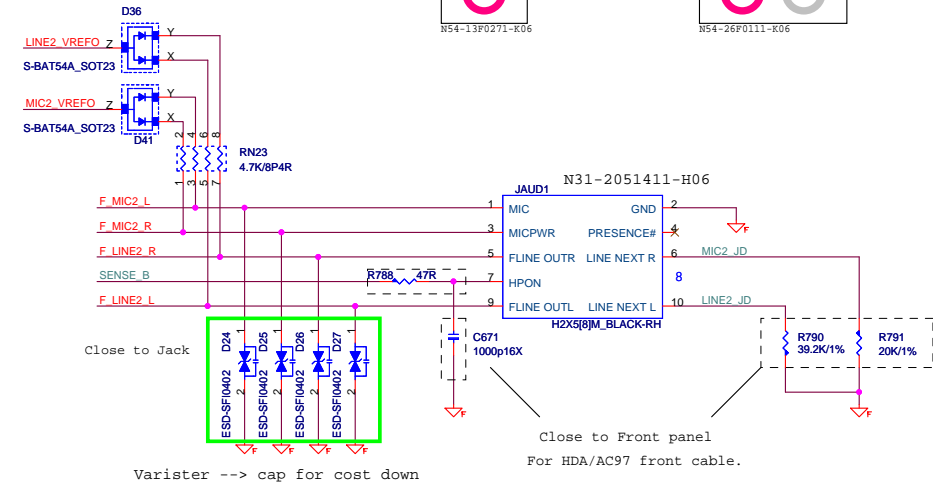
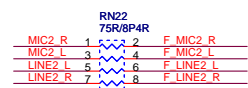
## ALC892



The diagram shows a differential amplifier circuit. The input is a differential-mode signal  $V_{in,dm}$  applied to the non-inverting input of the op-amp. The inverting input is connected to a feedback network consisting of a resistor  $R_{f1}$  and a resistor  $R_{f2}$  in series, which is connected to the output. The output is connected to a load resistor  $R_L$  and a feedback resistor  $R_f$  in series, which is connected to the inverting input. The output voltage is  $V_{out}$ . The circuit is labeled with component values:  $R_{f1} = 22k$ ,  $R_{f2} = 22k$ , and  $R_f = 22k$ . The load resistor  $R_L$  is also  $22k$ . The input signal is  $V_{in,dm}$  and the output is  $V_{out}$ .



## 20111104 PM Remove



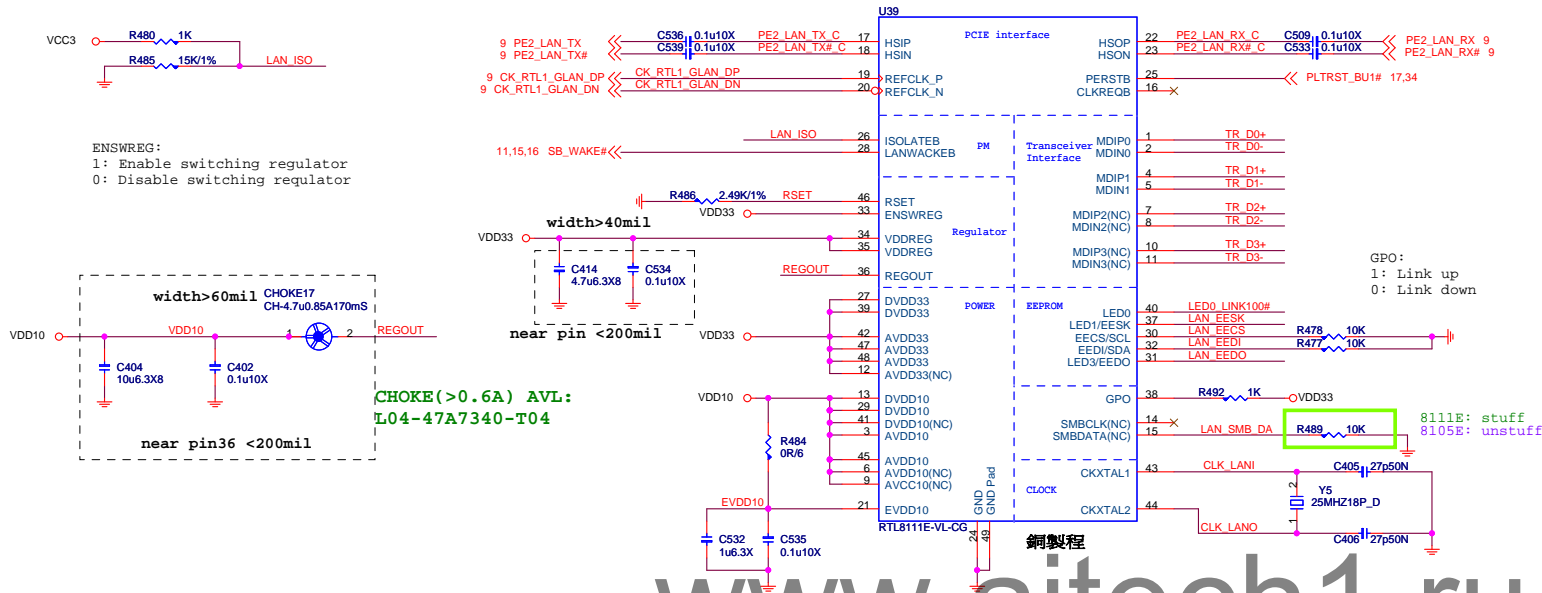
**MICRO-STAR INT'L CO.,LTD**

MS-7759

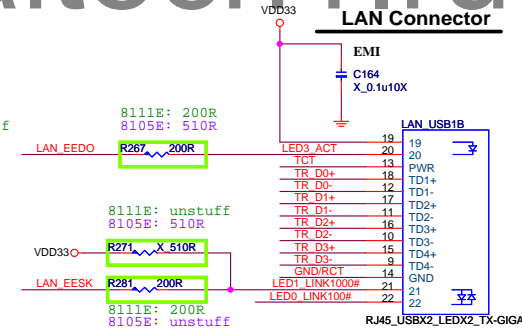
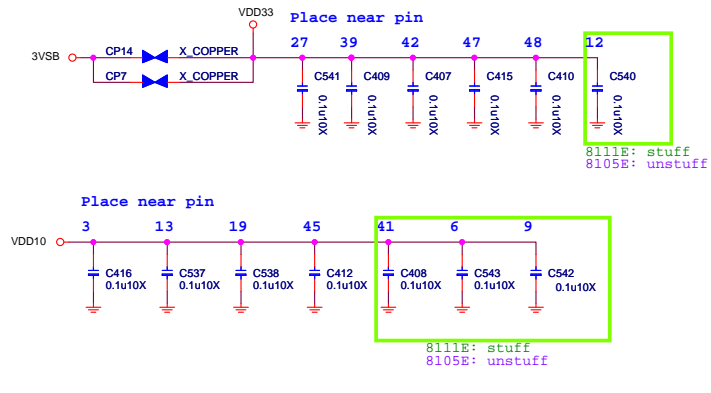
Size Custom	Document Description <b>Audio Codec ALC892/887</b>	Rev 1.0
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# RTL8111E Giga LAN

## RTL8105E 10/100M LAN



3.3v Power on rise time : 1-100ms. MAX: 163mA



only support LED0+LED1/LED1+LED3 dual color LED combinations when using EEPROM

8111E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

8105E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11

Giga-Lan	10/100-Lan
<b>N58-22F0731</b>	<b>N58-22F0771</b>
Link Yellow	Link Yellow
Active Blinking	Active Blinking
1000 Orange	1000 Orange
100 Green	100 Green
10 None	10 None
19	19
20	20
21	21
22	22

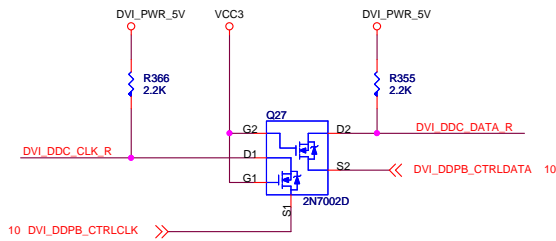
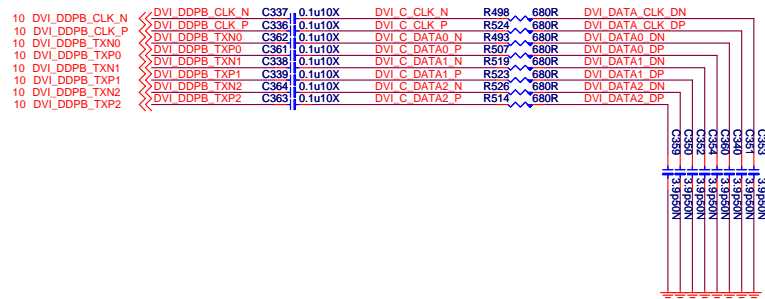


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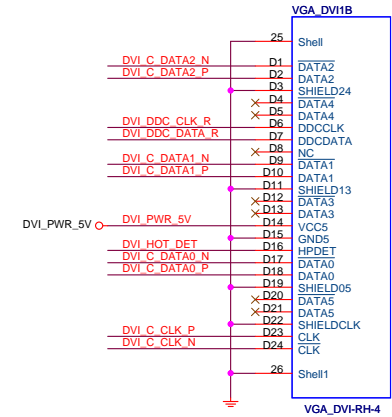
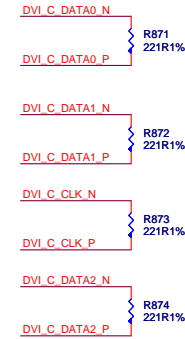
MS-7759

Size	Document Description	Rev
Custom	LAN-RTL8111E/8105E	1.0
Date: Wednesday, January 04, 2012	Sheet 19 of 41	

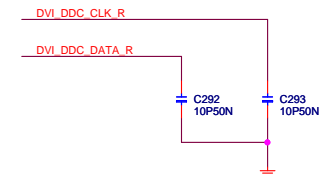
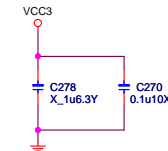
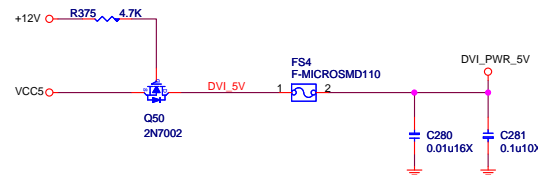
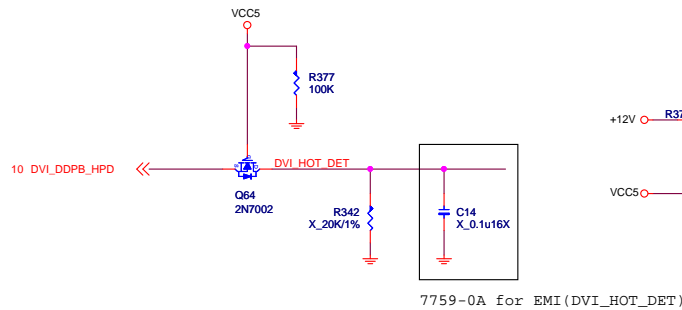
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



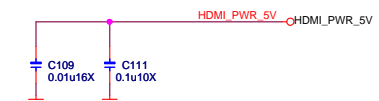
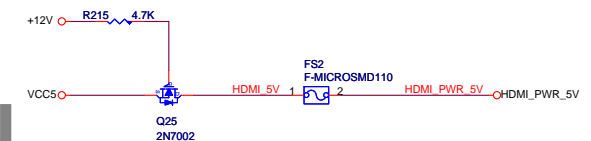
For EMI



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### ***+5V Power Signal***

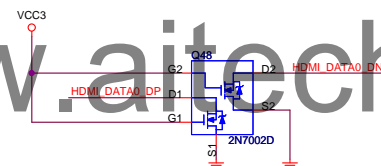
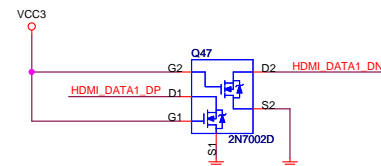
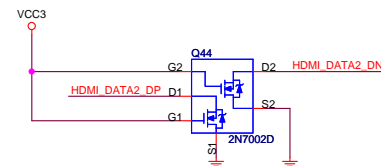
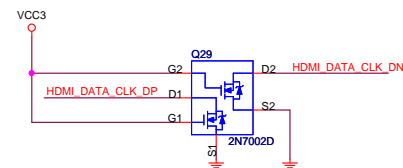
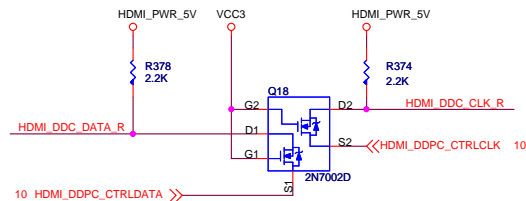
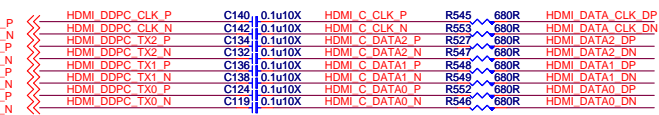
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HDMI DDC CLK R	C572	X 0.1u16X
HDMI DDC DATA R	C571	X 0.1u16X
HDMI HOT_DET	C570	X 0.1u16X



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Size Custom	Document Description <b>HDMI Connector</b>	Rev 1.0
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HDMI C\_CLK N R235 X\_180R/1%

HDMI C\_CLK P

HDMI C\_DATA0 N R225 X\_180R/1%

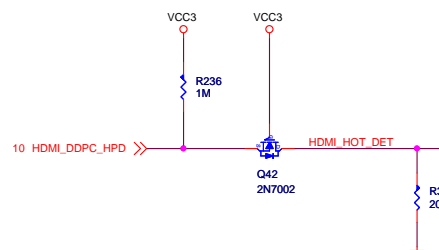
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HDMI C\_DATA1 N R233 X\_180R/1%

HDMI C\_DATA1 P

HDMI C\_DATA2 N R231 X\_180R/1%

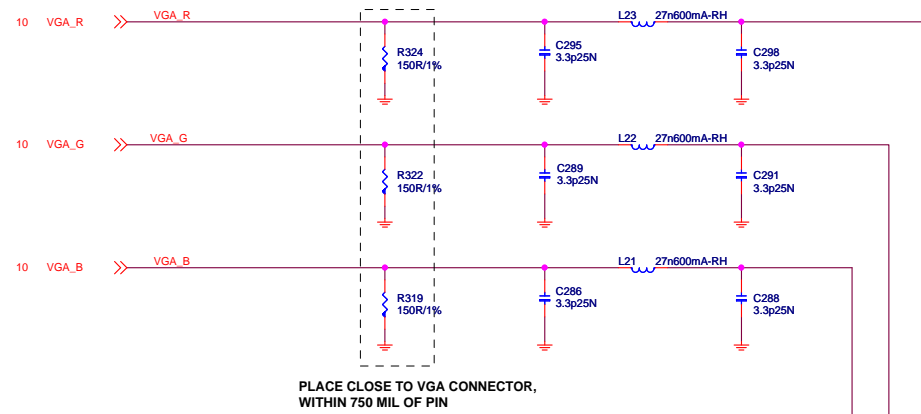
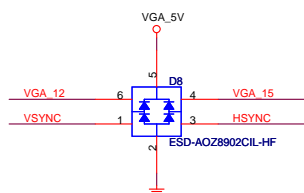
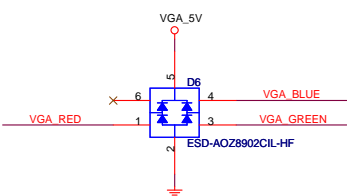
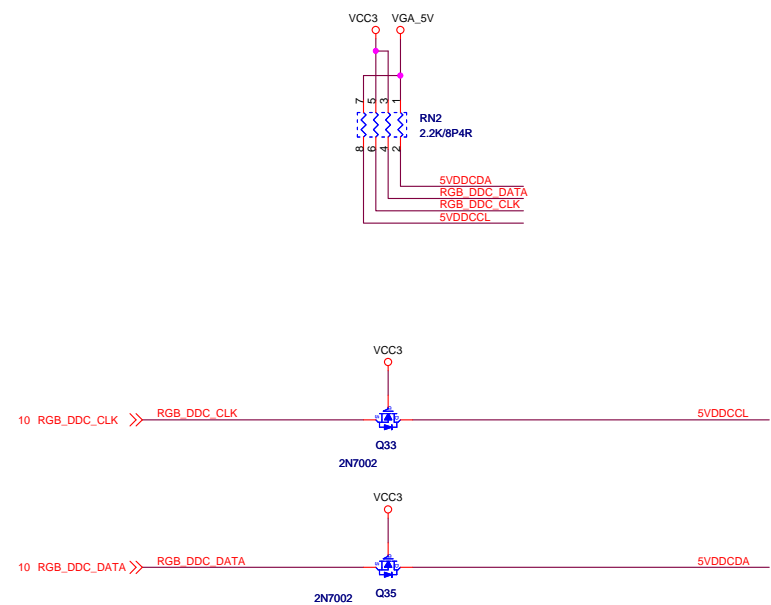
HDMI C\_DATA2 P



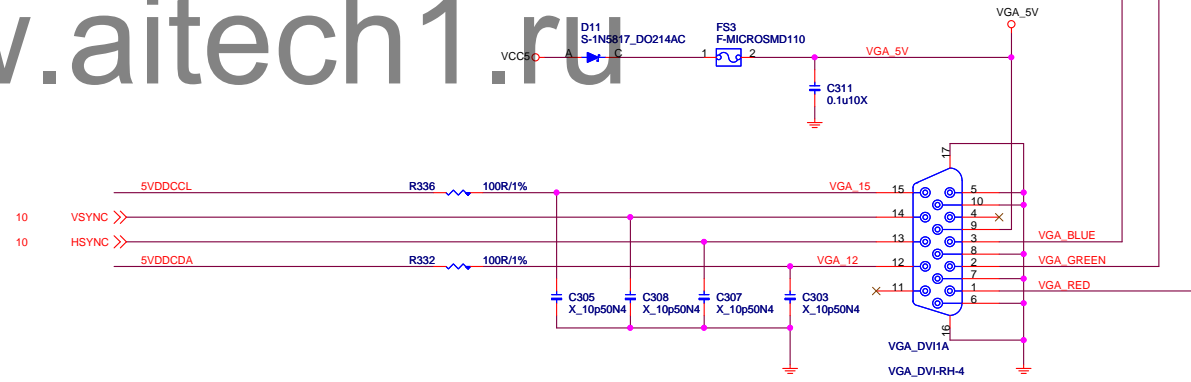
D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

Level shift



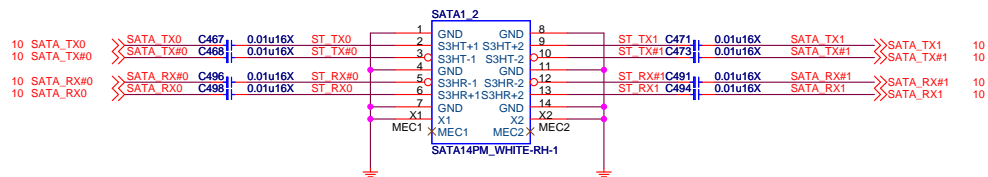
PLACE CLOSE TO VGA CONNECTOR,  
WITHIN 750 MIL OF PIN



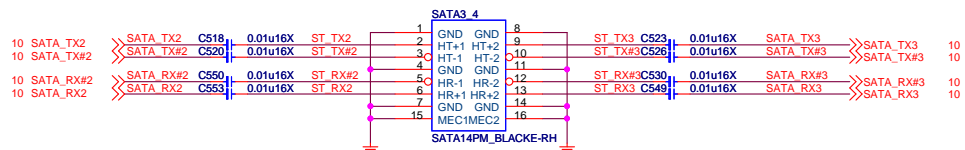
## SATA1-2

3.0

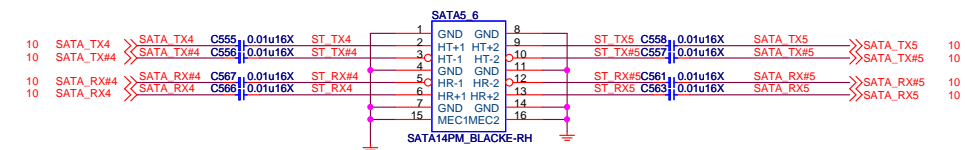
white



## SATA3-4



## SATA5-6



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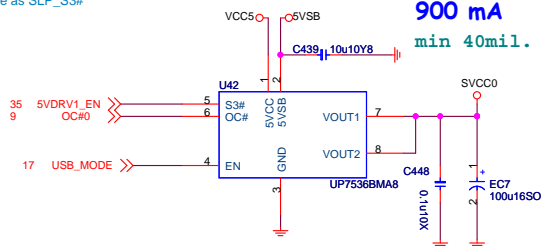
MS-7759

Size	Document Description	Rev
Custom	SATA Connector	1.0
Date: Wednesday, January 04, 2012		
Sheet 23 of 41		

## FRONT USB30 PORT 0,1

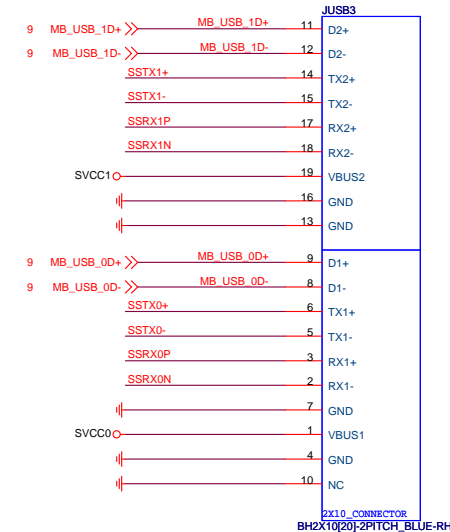
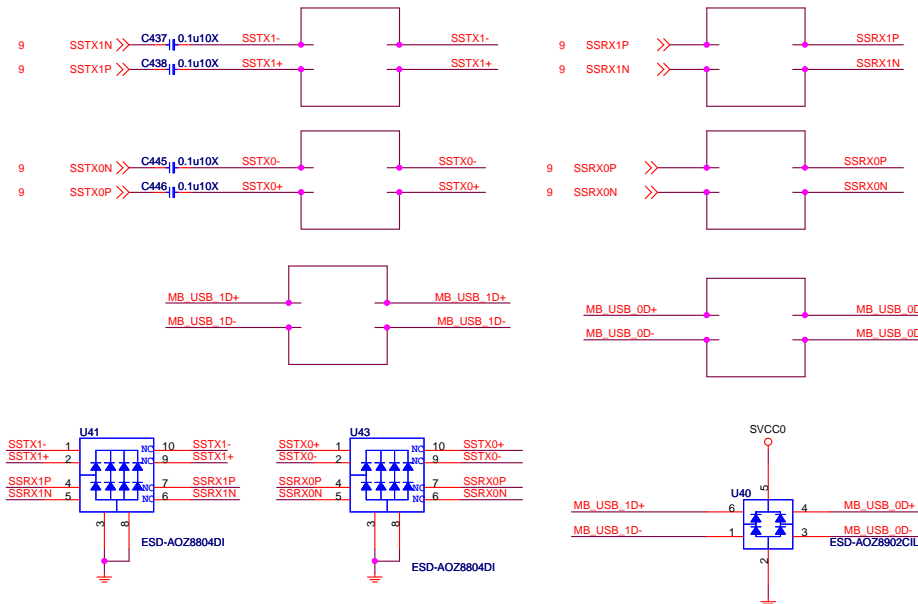
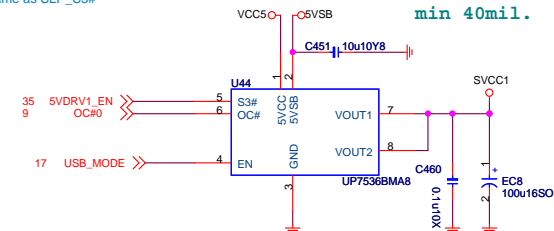
Same as SLP\_S3#

900 mA  
min 40mil.



Same as SLP\_S3#

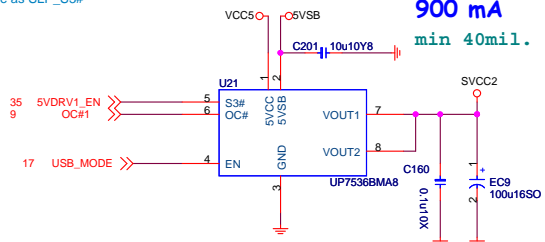
900 mA  
min 40mil.



## REAR USB30 PORT 2,3

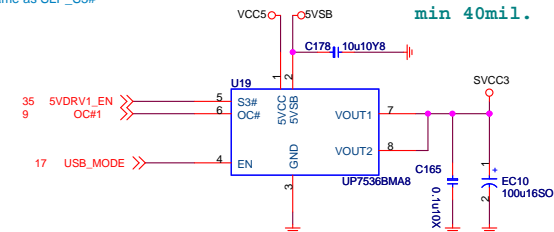
Same as SLP\_S3#

900 mA  
min 40mil.



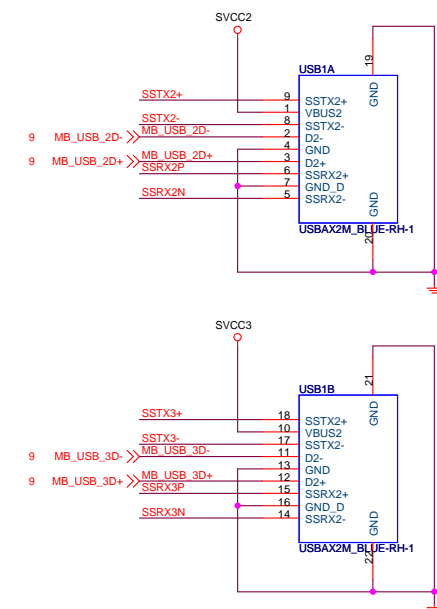
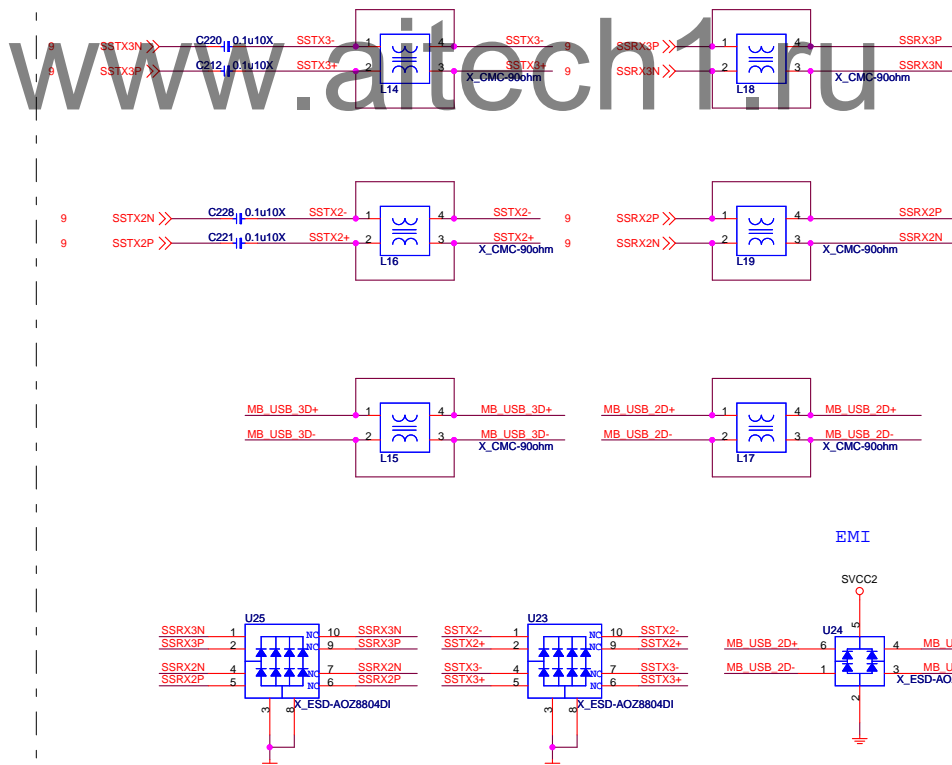
Same as SLP\_S3#

900 mA  
min 40mil.



USB\_MODE  
Hi by BIOS programming,  
default h/w PD for avoid UP7536 Enable pin floating

USB_MODE States				
MODE	G3	S4/S5	S0	S3
EUP Disable	0	0	1	1
EUP Enable	0	0	1	1



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Custom	USB3.0 Connector	1.0
Date: Wednesday, January 04, 2012	Sheet 24 of 41	

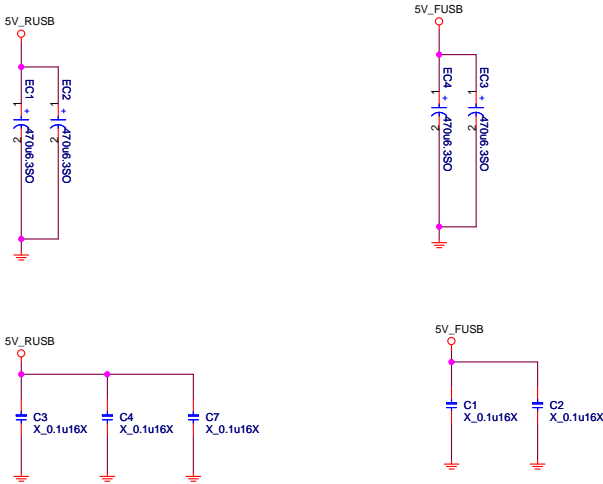
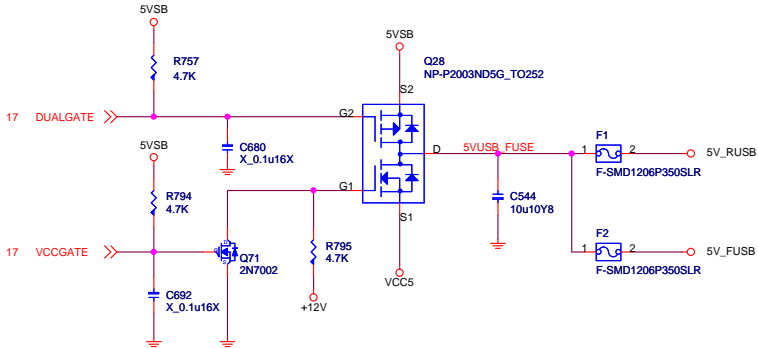
USB2.0/PS2 POWER Control			
MODE	S5	S0	S3
S3P5_Gate#	0/1	1	0
S0P5_Gate#	1	0	1

When PS2 in S5 not support wake , S3P5\_Gate# in S5 must setting to High

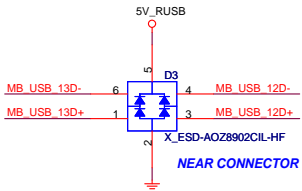
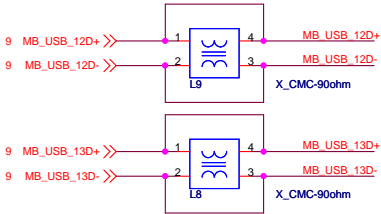
When PS2 in S5 support wake , S3P5\_Gate# in S5 must setting to Low

\*In S5# ( S3P5\_Gate # pin status is Tri-state, and can be programmed Low level.

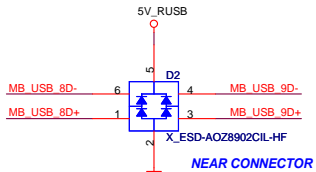
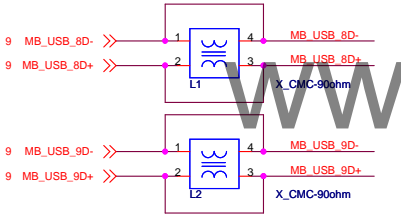
\*S3P5\_Gate# and S0P5\_Gate# can't setting to low together, avoid leakage voltage issue



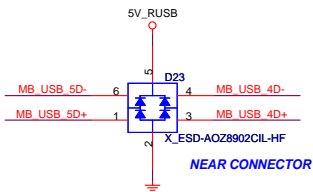
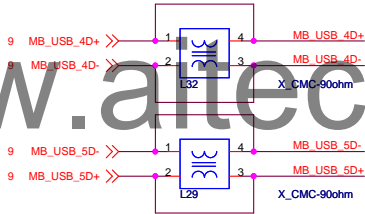
REAR USB PORT 8,9 (With LAN)



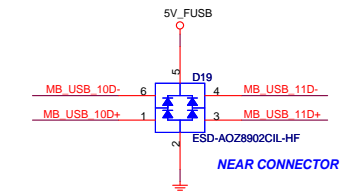
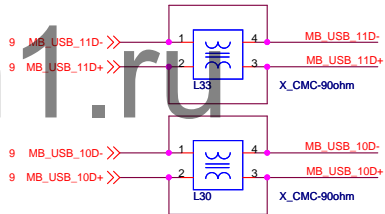
REAR USB PORT 8,9 (With PS2)



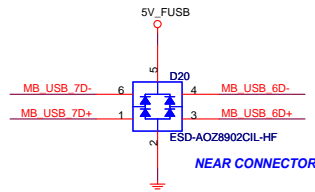
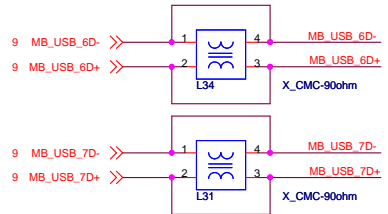
REAR USB PORT 8,9 (With HDMI)



FRONT USB PORT 0,1



FRONT USB PORT 8,9

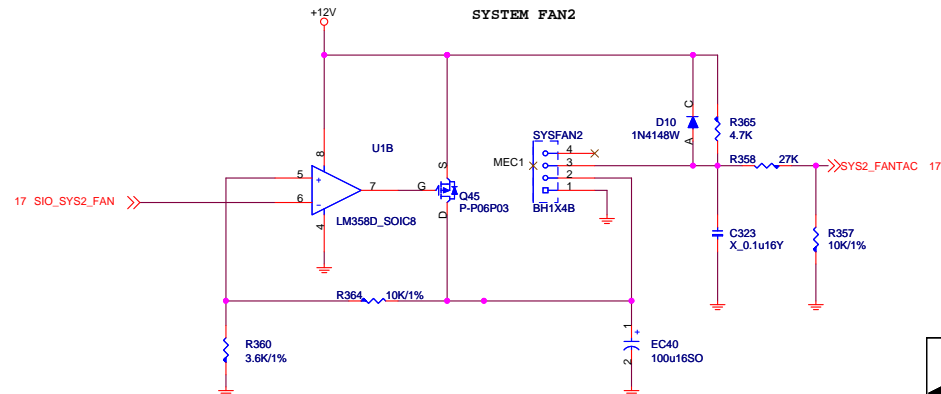
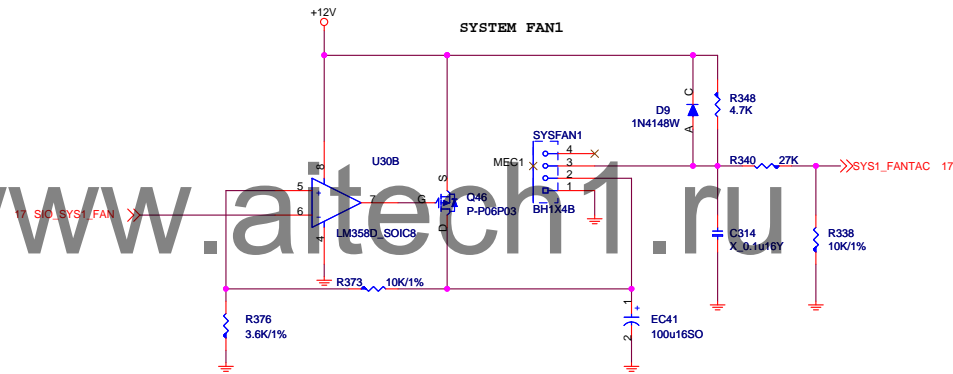
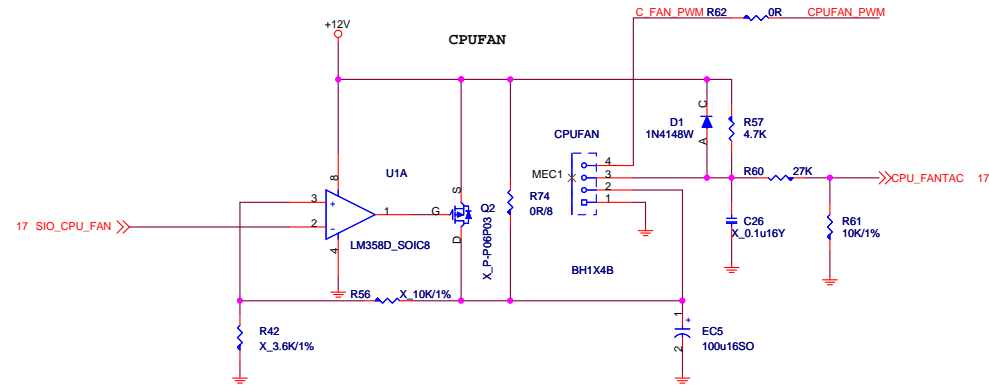
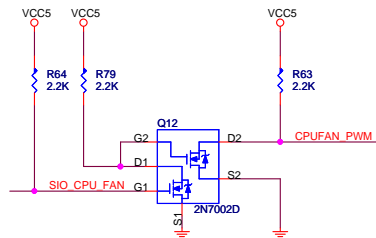


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Custom	Rear I/O & USB2.0 Connector	1.0
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# FAN-COUNTROL CIRCUIT



**VRMPWRGD LEVEL SHIFT**

CPU\_VTT, 3VSB, VCC3, VRM\_PGDR, VR\_HOT#, VID\_ALERT#, H\_VIDSCLK, H\_VIDSOUT, 3000mil < L < 6000mil, 4mil / 20mil, 55 ohm Impedance must be Referenced GND.

**CRB**

B1:0.63, B2:0.05, C1:0.05, C2:3.2, E1:0.05, E2:0.01

**UPI VOLTAGE CONSOLE**

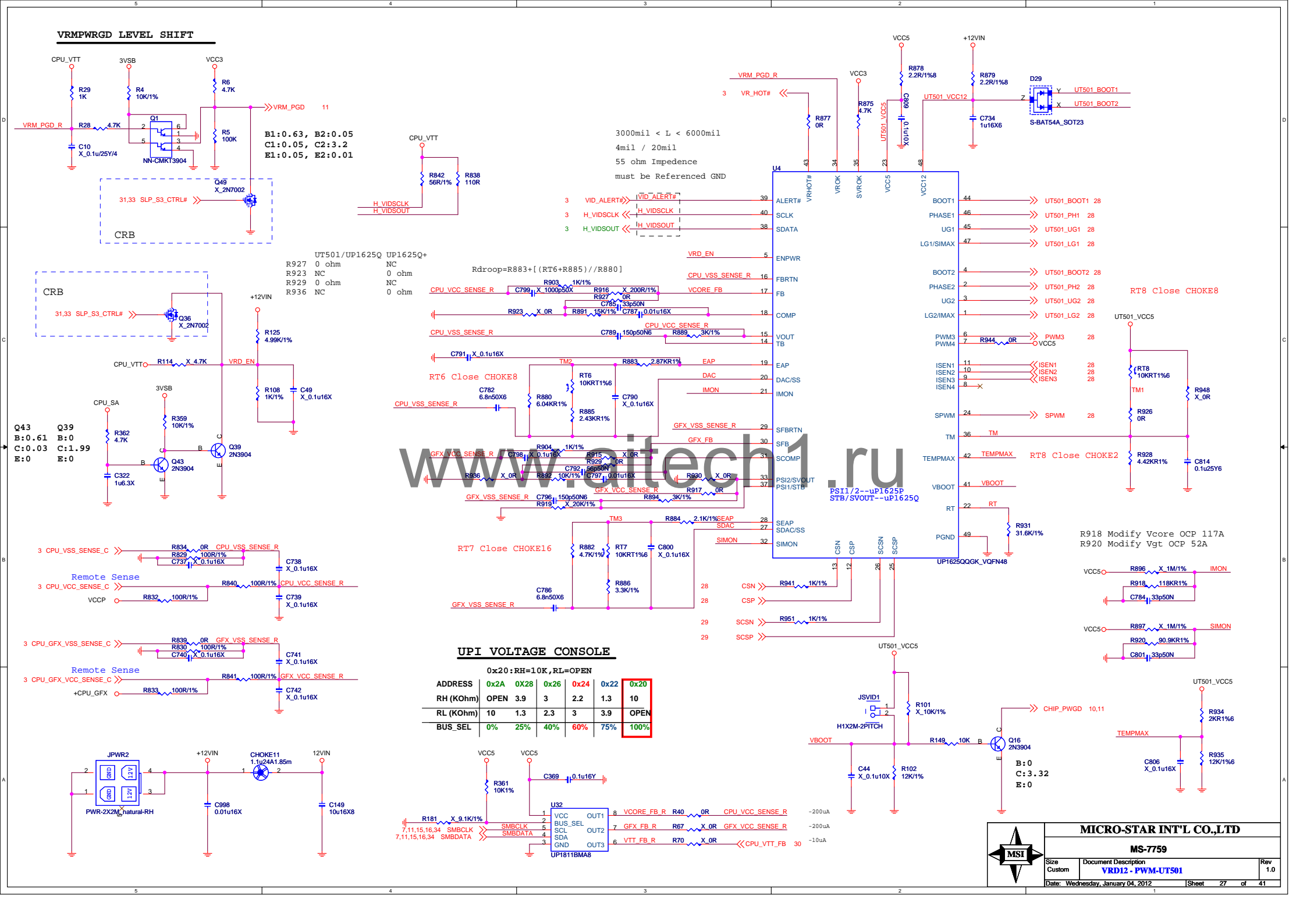
ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (Kohm)	OPEN	3.9	3	2.2	1.3	10
RL (Kohm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

**MICRO-STAR INT'L CO.,LTD**

**MS-7759**

Size Custom Document Description **VRD12 - PWM-UTS01** Rev 1.0

Date: Wednesday, January 04, 2012 Sheet 27 of 41



**VRMPWRGD LEVEL SHIFT**

CPU\_VTT, 3VSB, VCC3, VRM\_PGDR, VR\_HOT#, VID\_ALERT#, H\_VIDSCLK, H\_VIDSOUT, 3000mil < L < 6000mil, 4mil / 20mil, 55 ohm Impedance must be Referenced GND.

**UPI VOLTAGE CONSOLE**

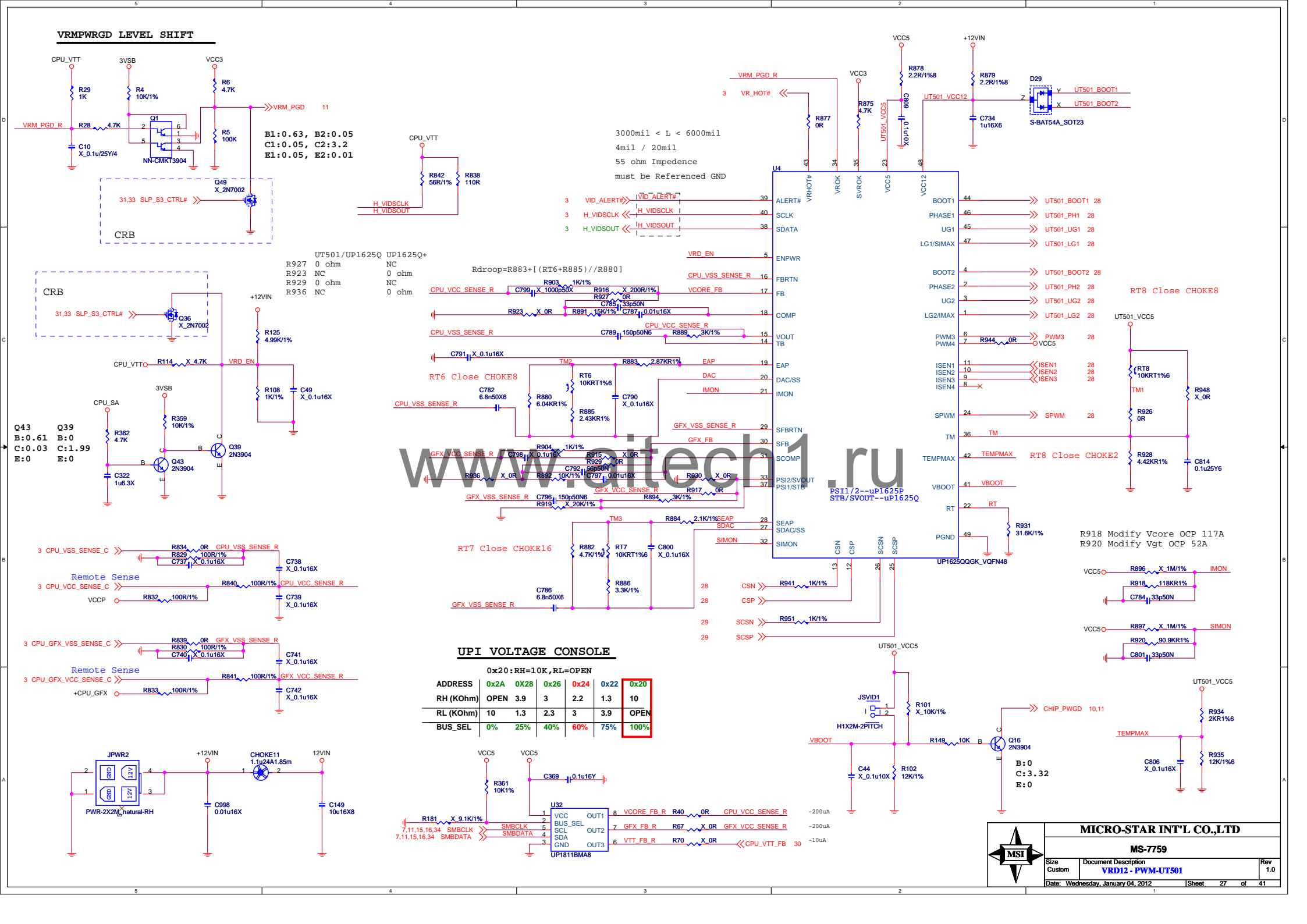
0x20 : RH=10K, RL=OPEN							
ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20	
RH (Kohm)	OPEN	3.9	3	2.2	1.3	10	
RL (Kohm)	10	1.3	2.3	3	3.9	OPEN	
BUS_SEL	0%	25%	40%	60%	75%	100%	

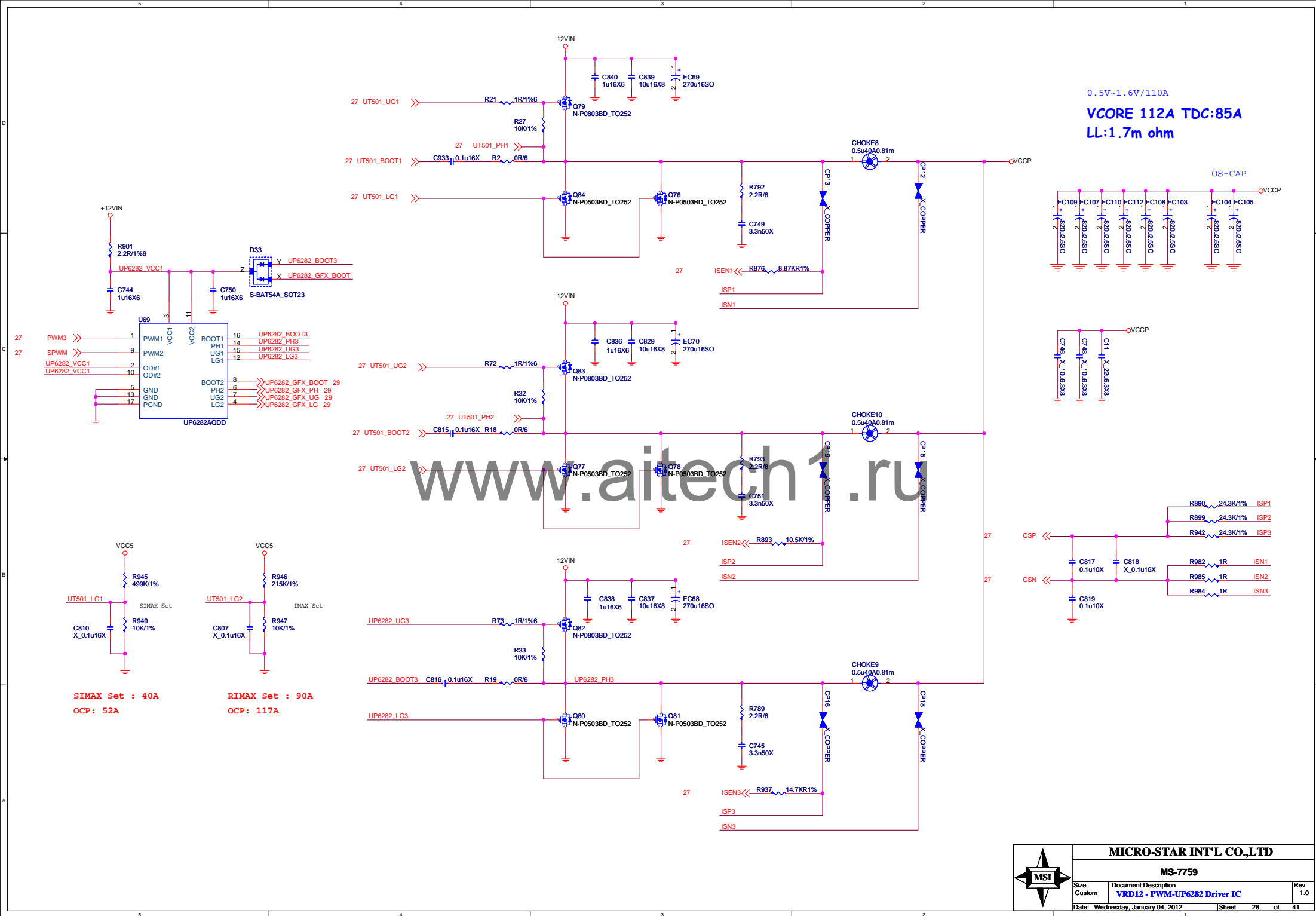
**MICRO-STAR INT'L CO.,LTD**

**MS-7759**

Size Custom Document Description **VRD12 - PWM-UTS01** Rev 1.0

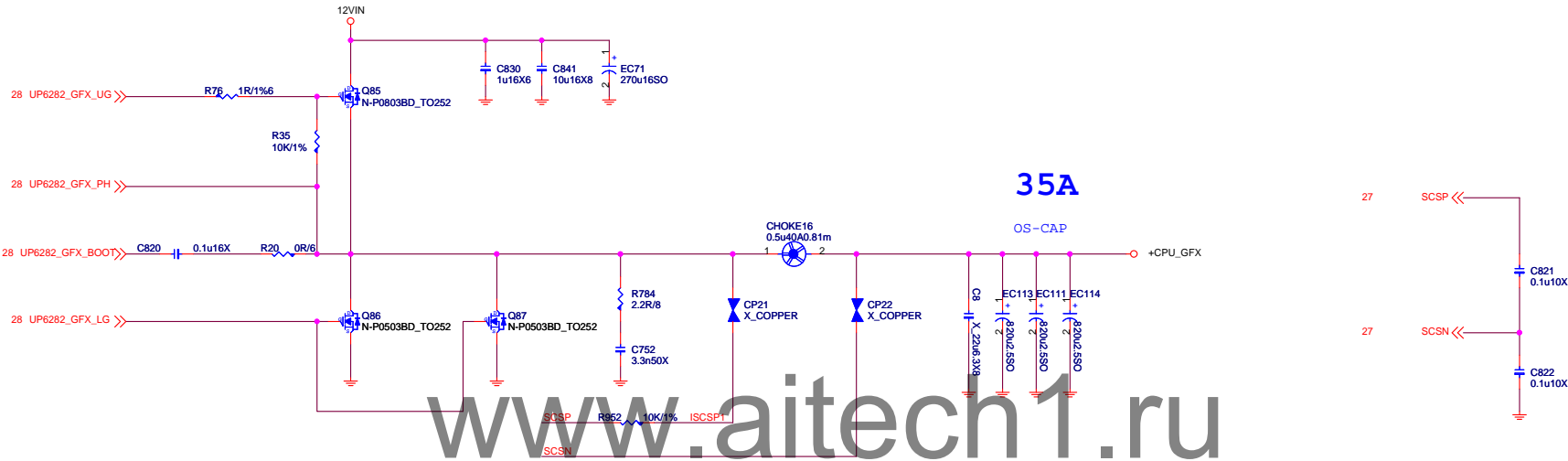
Date: Wednesday, January 04, 2012 Sheet 27 of 41





CPU\_GFX:0.25-1.52

35A FOR CPU

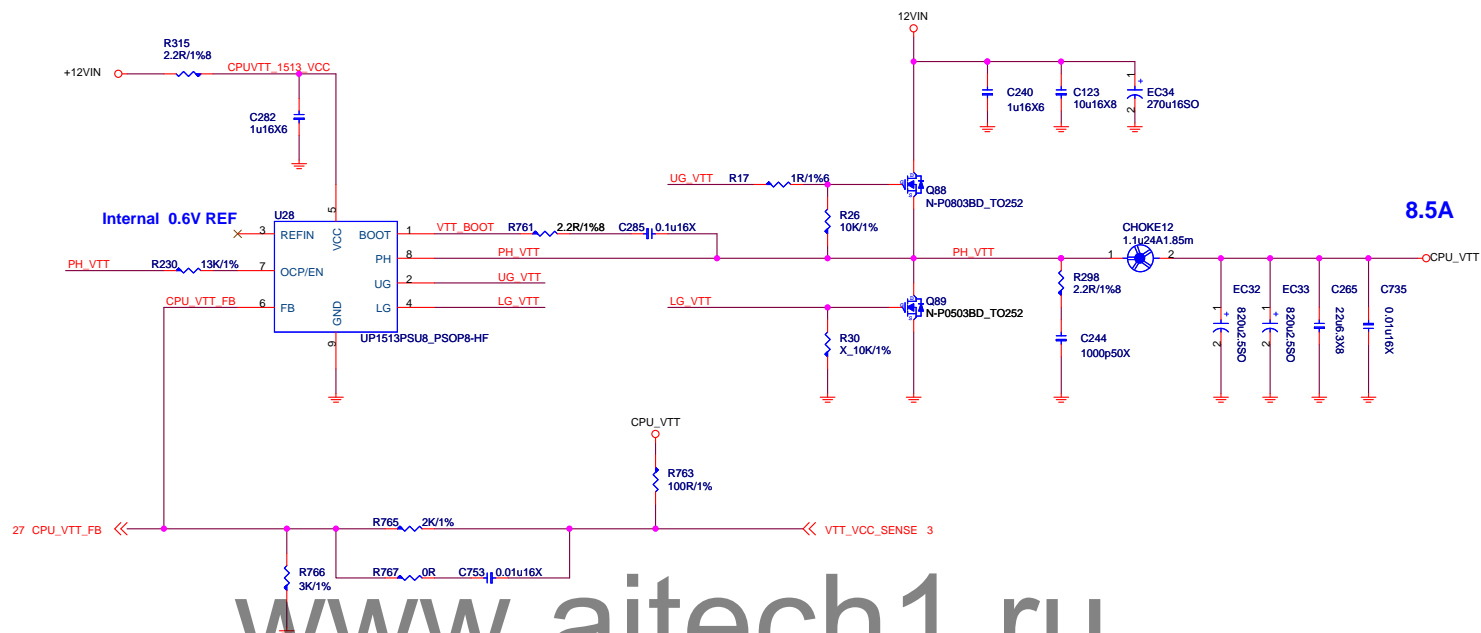


CPU\_VTT:1.05/1.00 MAX 17.3A

CPU VTT 8.5A SA Core =8.8A

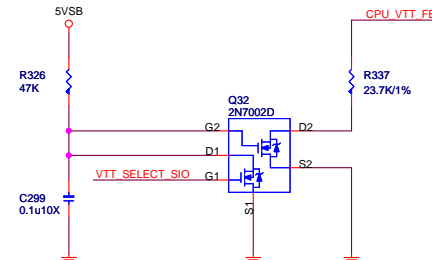
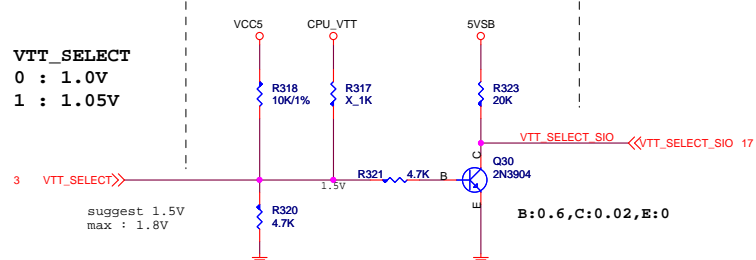
8.5A FOR CPU

$I_{ripple} = 1.92(vtt) + 1.88(sa)$   
 $5 * 1 = 5A > 3.8A$



VTT_SELECT	
Low	1.0V
High	1.05V

VTT_SELECT Table	
Low	1.05V
High	1.0V



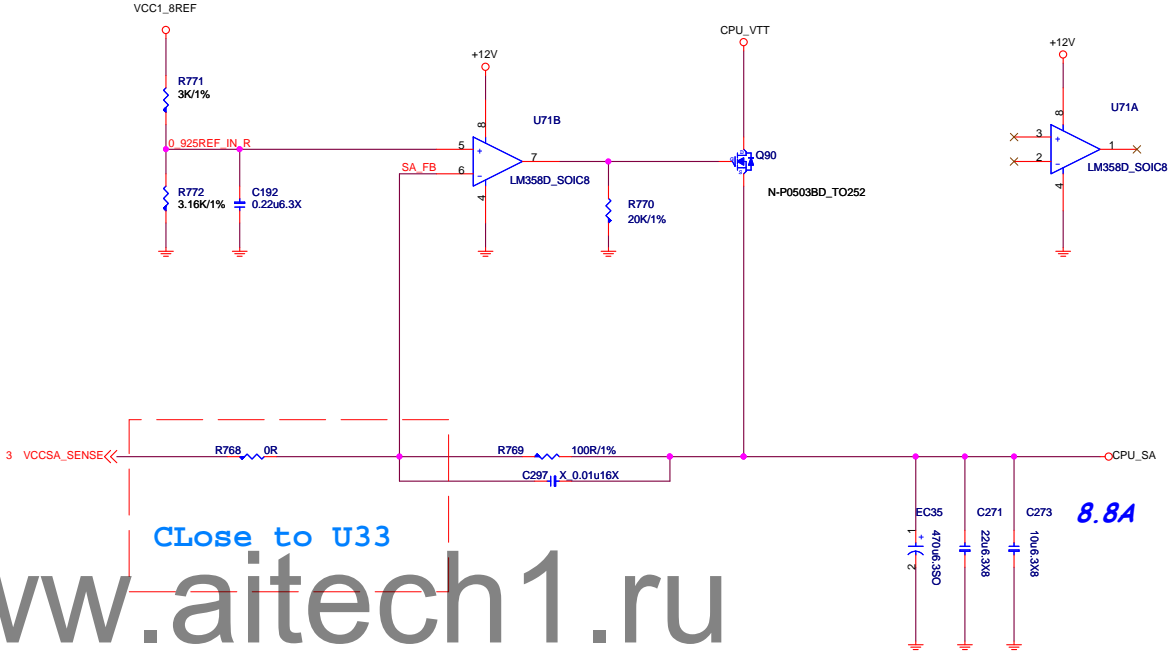
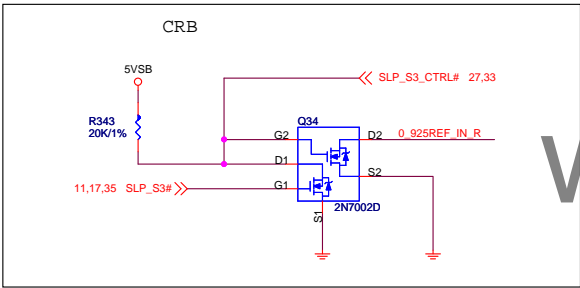
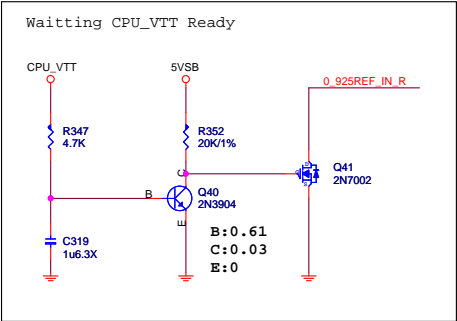
MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	VTT POWER- uP1513- 1Phase MOS	1.0
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CPU\_SA:0.925/0.85

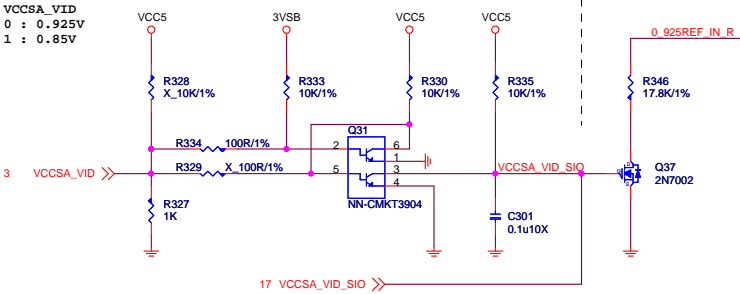
SA Core =8.8A



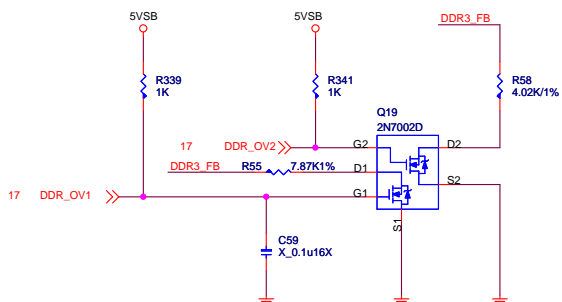
VCCSA_VID	
Low	0.925V
High	0.85V

VCCSA_VID_SIO Table	
Low	0.925V
High	0.85V

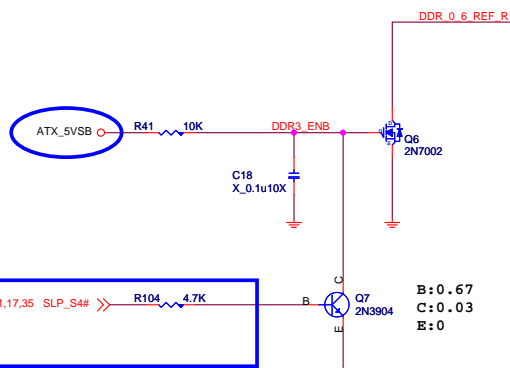
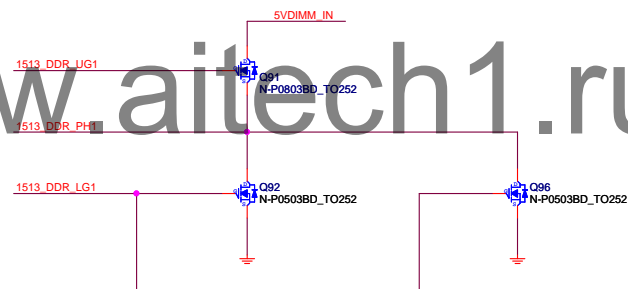
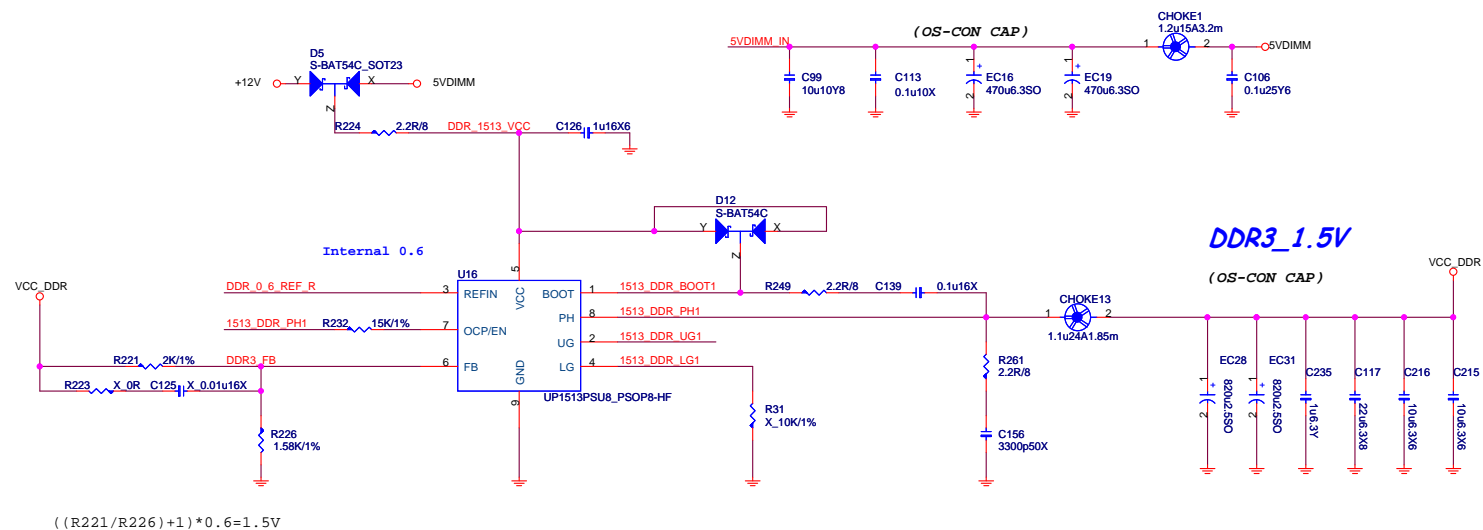
B1:0.33, B2:0.65  
C1:0.65, C2:0.01  
E1:0, E2:0



4.75A FOR CPU  
15A FOR 4DIMM  
1A FOR DDR VTT



```
DDR_OV1 = GPIO01(S/IO)
DDR_OV2 = GPIO02(S/IO)
```



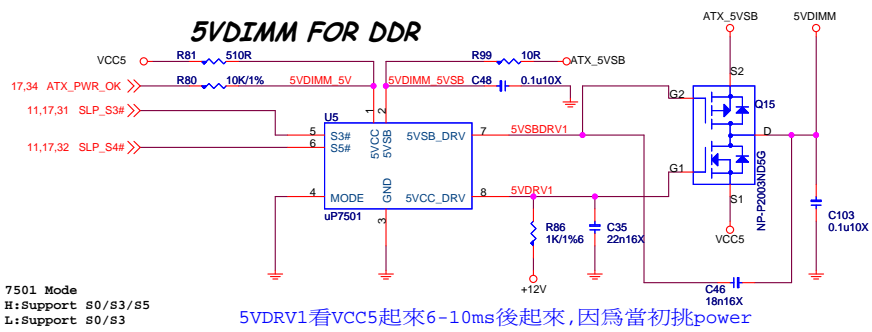
Size Custom	Document Description <b>DDR Power -UP1513 1-Phase MOS</b>	Rev 1.0
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**1.8A FOR ME CORE**

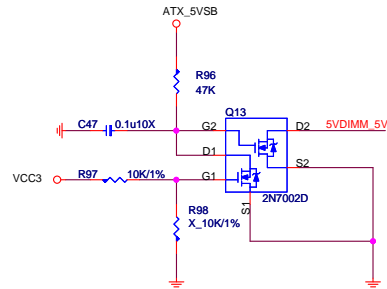
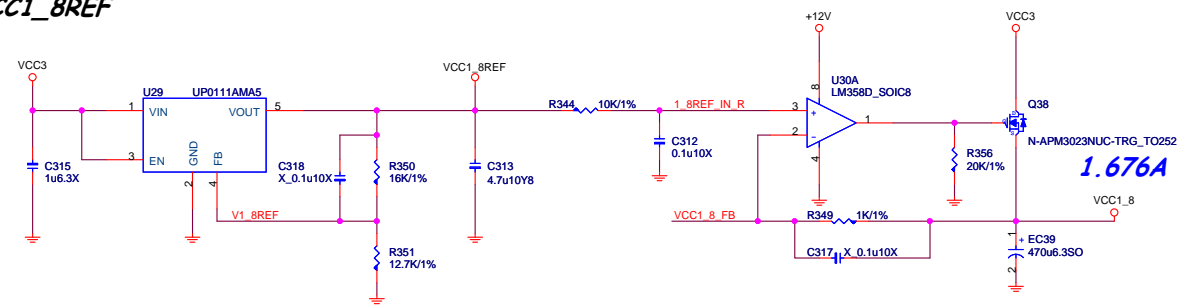




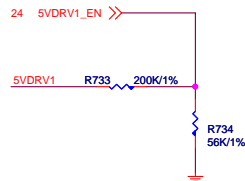
## 5VDIMM FOR DDR



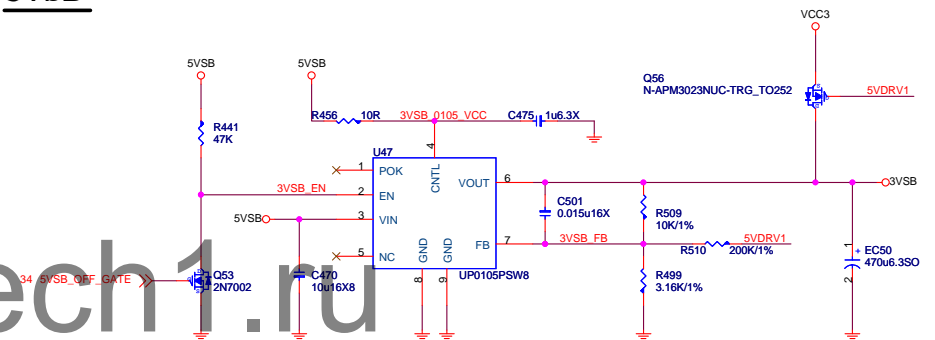
## VCC1\_8REF



## USB MODE

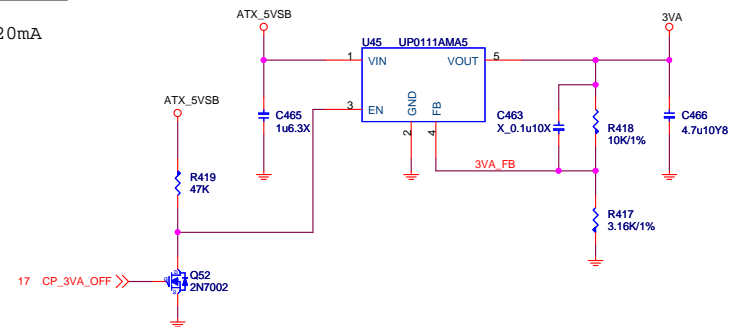


## 3VSB



## 3VA

20mA



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Custom	ACPI controller UPI	1.0
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MS-7759-0A

OPT	Configure	BOM	Function
	Z77MA-G45	601-7759-A10	MS-7759-0A Z77MA-G45 4*DDR3 + 2*PCI-Ex16 + 2*PCI-Ex1 + 4*SATAII + 2*SATAIII + 10*USB2.0 + 4*USB3.0 + HD 8Ch Audio + HDMI + DVI + Gb LAN All solid CAP,EuP,RoHS

Voltage test point

VCCP		VCCP
+CPU_GFX		+CPU_GFX
CPU_VTT		CPU_VTT
CPU_SA		CPU_SA
VCC_DDR		VCC_DDR
VTT_DDR		VTT_DDR
PCH_1P05		PCH_1P05
VCC1_8		VCC1_8
5VDIMM		5VDIMM
+12V		+12V
VCC5		VCC5
VCC3		VCC3
ATX_5VSB		ATX_5VSB
5VSB		5VSB
3VSB		3VSB
VBAT		VBAT
3VA		3VA

PCB1  
7759\_10

PK0-0775910-G37, 精成, 23, 寶安恩斯通廠 (MSIS)  
PK0-0775910-G37, 精成, 27, 寶安恩斯通廠 (MSIS)  
PK0-0775910-E48, 競華, 23, 寶安恩斯通廠 (MSIS)  
PK0-0775910-E48, 競華, 27, 寶安恩斯通廠 (MSIS)

Z77MA-G45  
Label  
601-7759-XXX  
MKT-LABEL

HDMI\_LA1  
Real Label  
HDMI  
HDMI\_LRA  
HDMI Label P/N

HDMI\_LA1  
Label  
HDMI  
HDMI\_LABEL  
Virtual MSI P/N

LA1  
AMI BIOS  
LABEL  
BIOS\_LABEL

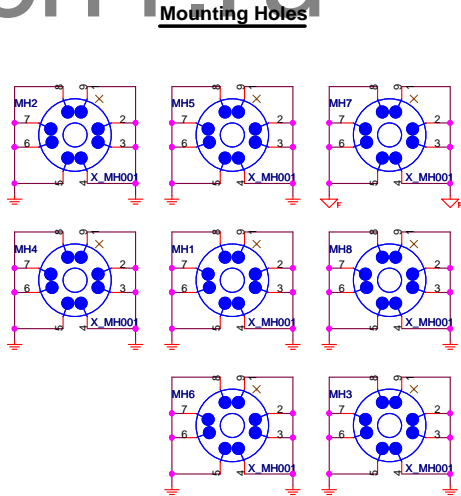
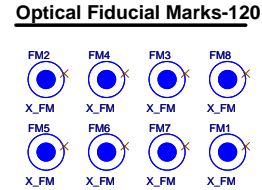
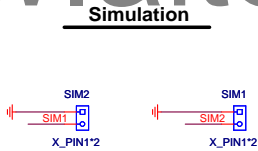
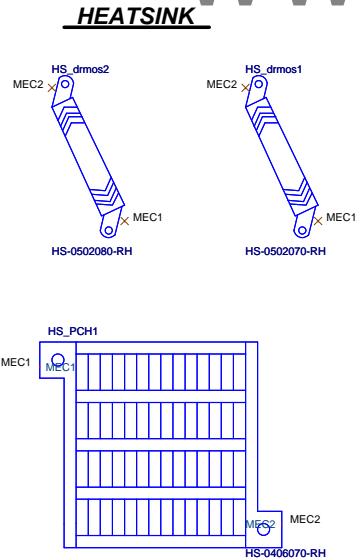
LABEL1  
X\_BUY

BAT1\_X1  
BAT-BCR2032P-RH

LABEL2  
X\_BUY

CPU\_H1  
CPU  
鐵座  
CPU\_H1

THX\_LA2  
Label  
THX  
THX LABEL



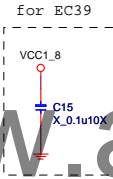
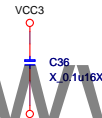
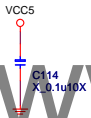
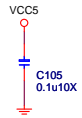
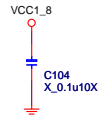
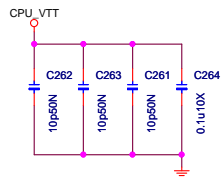
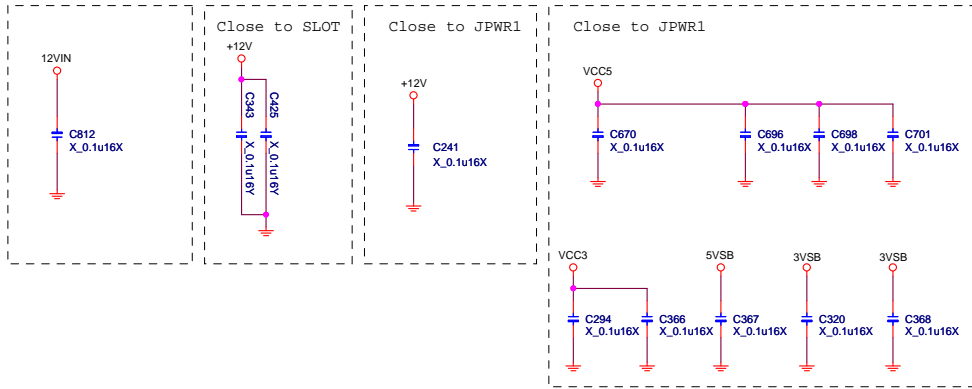
MSI

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